DECLARATION

I, Shinichi Usui, a Japanese Patent Attorney registered No.09694, of Okabe International Patent Office at No. 602, Fuji Bldg., 2-3, Marunouchi 3-chome, Chiyoda-ku, Tokyo, Japan, hereby declare that I have a thorough knowledge of Japanese and English languages, and that the attached pages contain a correct translation into English of the priority documents of Japanese Patent Application No. 7-260100 filed on October 6, 1995 in the name of CANON KABUSHIKI KAISHA.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made, are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 10th day of February, 2004

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PATENT OFFICE
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Date of Application: October 6, 1995

Application Number: Japanese Patent Application No. 7-260100

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November 1, 1996

Commissioner,
Patent Office TOSHIMITSU ARAI (Seal)

Certificate No. 08-3077119

[Name of the document] Patent Application

[Reference No.] 3122001

[Date] October 6, 1995

[Addressed to] Commissioner, Patent Office
YUJI KIYOKAWA

[International Classification] H01L 21/20

[International Classification] G30B 19/00

[Title of the Invention] SEMICONDUCTOR SUBSTRATE AND PROCESS FOR PRODUCING SAME

[Number of the Claims] 35

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[Indication of Official Fee]

[Way of Payment] Prepaid

[Prepayment Ledger No.] 011224

[Amount] 21000

[List of Filed Materials]

[Material] Specification 1

[Material] Drawings 1

[Material] Abstract 1

[General Power of Attorney] 9003707

[Proof Requirement] Required

[Name of the Document] Specification

[Title of the Invention] Semiconductor Substrate and Process for Producing Same

[What is Claimed is]

[Claim 1] A semiconductor substrate comprising a porous Si layer as a surface layer of at least one main plane side of an Si substrate and a porous Si layer having a thin pore wall included in said porous Si layer.

[Claim 2] A semiconductor substrate comprising a porous Si layer as a surface layer of at least one main plane side of an Si substrate and a porous Si layer having a high porosity included in said porous Si layer.

[Claim 3] The semiconductor substrate according to claim 1, wherein said porous Si layer having a thin pore wall is present in a region located at a constant depth from the surface of said porous Si layer.

[Claim 4] The semiconductor substrate according to claim 2, wherein said porous Si layer having a high porosity is present in a region located at a constant depth from the surface of said porous Si layer.

[Claim 5] A process for preparing a semiconductor substrate comprising the steps of rendering the surface layer of at least one main plane side of an Si substrate porous, and ion implanting at least one element of rare gases, hydrogen and nitrogen into the porous Si layer with a given projection range.

[Claim 6] A semiconductor substrate totally

comprising porous Si in a thickness direction and having a total film thickness 20 μm or less.

[Claim 7] A process for preparing a semiconductor substrate comprising the steps of rendering the surface layer of at least one main plane side of a first Si substrate porous, ion implanting at least one element of rare gases, hydrogen and nitrogen with a projection range in said porous layer, and separating the semiconductor substrate into two in said porous Si.

[Claim 8] The process for preparing a semiconductor substrate according to claim 7, wherein said separation in the porous Si is conducted using at least one method from the group consisting of heat-treatment of said Si substrate, application of pressure to said Si substrate in a direction perpendicular to the surface thereof, drawing said Si substrate in a direction perpendicular to the surface thereof and application of shearing stress to said Si substrate.

[Claim 9] A semiconductor substrate comprising a non-porous thin film on a porous Si layer of at least one main plane side of a semiconductor substrate and a porous layer having a pore wall thinner than that of other porous portion, included in said porous Si layer.

[Claim 10] A semiconductor substrate comprising a non-porous thin film on a porous Si layer at least one main plane side of a semiconductor substrate and a porous layer having a porosity higher than that of other porous

portion, included in said porous Si layer.

[Claim 11] A process for preparing a semiconductor substrate comprising the steps of rendering the surface of at least one main plane side of a first Si substrate porous, forming a non-porous thin film on said porous Si layer, and ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous Si layer with a given projection range.

[Claim 12] The process for preparing a semiconductor substrate according to claims 9 to 11, wherein said non-porous thin film is made of single-crystal silicon.

[Claim 13] A process for preparing a semiconductor substrate comprising the steps of bonding the main plane of a first Si substrate having a non-porous thin film formed on a porous Si layer to the main plane of a separately prepared second substrate, separating the bonded substrate at the porous Si layer, and selectively removing the porous layer exposed on the surface of the second substrate.

[Claim 14] A process for preparing a semiconductor substrate comprising the steps of rendering the surface layer of a main plane side of a first Si substrate porous, forming a non-porous layer on said porous Si layer, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layer with a given projection range, bonding the main plane of said first Si

substrate to a main plane of second substrate, separating the bonded substrate at said porous Si layer, and selectively removing the porous layer exposed on the surface of the second substrate.

[Claim 15] A process for preparing a semiconductor substrate comprising the steps of rendering the surface layer of a main plane side of a first Si substrate porous, forming a non-porous layer on said porous Si layer, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layer with a given projection range, bonding said first Si substrate to a main plane of a second substrate, separating the bonded substrate at said porous Si layer, selectively removing the porous Si layer exposed on the surface of the second substrate, again forming a non-porous layer on the porous silicon layer exposed on the surface of the first substrate, and ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layer with a given projection range.

[Claim 16] A process for preparing a semiconductor substrate comprising the steps of rendering the surface layers located at two main plane sides of a first Si substrate porous, forming a non-porous layer on each of said porous Si layers of the two main planes, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layers of said two main planes with a given projection range, bonding each of the

two main planes respectively to each main plane of separately prepared two support substrates, separating the bond substrate into three at said porous Si layers, and selectively removing said porous Si layer exposed on the surfaces of said two support substrates.

[Claim 17] A process for preparing a semiconductor substrate comprising the steps of rendering the surface layers located at two main sides of a first Si substrate porous, forming a non-porous layer on each of said porous Si layers of the two main planes, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layers of said two main planes with a given projection range, bonding each of the two main planes respectively to each main plane of separately prepared two support substrates, separating the bonded wafer into three at said porous Si layers, selectively removing said porous Si layer exposed on the surfaces of said two support substrate, and removing said porous Si layer remained on the first substrate.

[Claim 18] A process for preparing a semiconductor substrate comprising the steps of rendering the surface layers located at two main plane sides of a first Si substrate porous, forming a non-porous layer on each of said porous Si layers of the two main planes, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layers of said two main planes with a given projection range, bonding each of the

two main planes respectively to each main plane of separately prepared two support substrates, separating the bonded wafer into three at said porous Si layers, selectively removing said porous Si layer exposed on the surfaces of said two support substrates, again forming a non-porous layer on the porous silicon layer exposed on the surface of the first Si substrate, and ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layer with a given projection range.

[Claim 19] The process for preparing a semiconductor substrate according to claims 13 to 18, wherein said separation at said porous Si layer is conducted using at least one method from heating-treatment of the bonded substrate, application of pressure to the bonded substrate in a direction perpendicular to the surface thereof, drawing the bonded substrate in a direction perpendicular to the surface thereof and application of shearing stress to the bonded substrate.

[Claim 20] The process for preparing a semiconductor substrate according to claims 13 to 18 further comprising a step of flattening the surface of the substrate after said porous Si layer removing step.

[Claim 21] The process for preparing a semiconductor substrate according to claim 20, wherein said surface flattening step is conducted by heat-treating under an atmosphere containing hydrogen.

[Claim 22] The process for preparing a semiconductor substrate according to claims 13 to 21, wherein said non-porous layer is a single-crystal Si layer.

[Claim 23] The process for preparing a semiconductor substrate according to claims 13 to 21, wherein said non-porous layer comprises an oxidized silicon layer and a single-crystal Si layer.

[Claim 24] The process for preparing a semiconductor substrate according to claims 13 to 21, wherein said non-porous layer is a single-crystal compound semiconductor layer.

[Claim 25] The process for preparing a semiconductor substrate according to claims 13 to 24, wherein said support substrate is an Si substrate.

[Claim 26] The process for preparing a semiconductor substrate according to claims 13 to 24, wherein said support substrate is an Si substrate in which a silicon oxide film is formed on at least a main plane to be bonded.

[Claim 27] The process for preparing a semiconductor substrate according to claims 13 to 24, wherein said support substrate is a light transmissible substrate.

[Claim 28] The process for preparing a semiconductor substrate according to claims 16 to 21, wherein said two support substrates are selected from an

Si substrate and a light transmissible substrate.

[Claim 29] The process for preparing a semiconductor substrate according to claims 13 to 28, wherein said removal of porous Si layer is conducted by electroless wet chemical etching using any one of hydrofluoric acid, a mixed solution of hydrofluoric acid with addition of at least one of alcohol and aqueous hydrogen peroxide, buffered hydrofluoric acid, and a mixed solution of buffered hydrofluoric acid with addition of at least one of alcohol and aqueous hydrogen peroxide.

[Claim 30] The process for preparing a semiconductor substrate according to claim 24, wherein said removal of porous Si layer is conducted by selectively chemical etching the porous Si using an etchant having an etching speed to the porous Si faster than that of the compound semiconductor.

[Claim 31] The process for preparing a semiconductor substrate according to claims 13 to 30, wherein said removal of porous Si layer is conducted by selectively polishing the porous Si layer using said non-porous layer as a stopper.

[Claim 32] The process for preparing a semiconductor substrate according to claims 13 to 31, wherein said bonding step is conducted using anodic bonding, pressurization, heat-treatment or a combination thereof.

[Claim 33] The process for preparing a semiconductor substrate according to any of claims 5, 7 and 8, wherein said pores forming step is conducted by anodization.

[Claim 34] The process for preparing a semiconductor substrate according to claims 11 to 32, wherein said pores forming step is conducted by anodization.

[Claim 35] The process for preparing a semiconductor substrate according to claims 33 or 34, wherein said anodization is conducted in an HF solution.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Field of the Industrial Utilization]

The present invention relates to a semiconductor substrate and a producing method thereof. More specifically, the present invention relates to dielectric isolation or a producing method of a single-crystal semiconductor on an insulator and a single-crystal compound semiconductor on an Si substrate, and further relates to a producing method of a semiconductor substrate suitable for an electronic device or an integrated circuit formed at a single-crystal semiconductor layer.

[0002]

[Prior Art]

Formation of a single-crystal Si semiconductor layer

on an insulator is widely known as a silicon on insulator (SOI) technique and has been researched to a large extent since a device utilizing the SOI technique has a number of advantageous points which can not be achieved by a bulk Si substrate forming the normal Si integrated circuit. Specifically, for example, the following advantageous points can be achieved by employing the SOI technique:

1. Dielectric isolation is easy and high integration is possible;
2. Radiation resistance is excellent;
3. Floating capacitance is reduced and high speed is possible;
4. Well process can be omitted;
5. Latch-up can be prevented;
6. Fully depleted (FD) field effect transistor is achieved through film thickness reduction.

These are described in detail, for example, in the literature of Special Issue: "Single-crystal silicon on non-single-crystal insulators"; edited by G.W. Cullen, Journal of Crystal Growth, volume 63, no 3, pp 429-590 (1983).

[0003]

Further, over the past few years, the SOI has been largely reported as a substrate which realizes the high speed of a MOSFET and the low power consumption (IEEE SOI conference 1994). Since an element has an insulating

layer at its lower part when employing the SOI structure, an element separation process can be simplified as compared with forming an element on a bulk silicon wafer so that a device process can be shortened. Specifically, in addition to achieving the higher performance, reduction of the wafer cost and the process cost is expected in total as compared with a MOSFET or IC on bulk silicon.

[0004]

Particularly, the fully depleted (FD) MOSFET is expected to achieve the higher speed and the lower power consumption through improvement in driving force. In general, a threshold voltage (Vth) of a MOSFET is determined by the impurity concentration at a channel portion. On the other hand, in case of the FD MOSFET using the SOI, a depletion layer is also subjected to an influence of a film thickness of the SOI. Thus, for producing the large scale integrated circuits at the high yield, uniformity of the SOI thicknesses has been strongly demanded.

[0005]

On the other hand, a device on a compound semiconductor has the high performance, such as, high speed and luminescence, which can not be achieved by Si. Presently, such a device is normally formed in an epitaxial layer grown on a compound semiconductor substrate, such as a GaAs substrate.

[0006]

However, there is a problem that the compound semiconductor substrate is expensive while low in mechanical strength so that the large area wafer is difficult to be produced.

[0007]

Under these circumstances, an attempt has been made to achieve the heteroepitaxial growth of a compound semiconductor on an Si wafer which is inexpensive and high in mechanical strength so that the large area wafer can be produced.

[0008]

The researches on formation of the SOI substrates have been active since the 1970s. In the beginning, the researches were well performed in connection with the SOS (sapphire on silicon) method which achieves the heteroepitaxial growth of single-crystal silicon on a sapphire substrate being an insulator, the FIPOS (fully isolation by porous oxidized silicon) method which forms the SOI structure by dielectric isolation based on oxidation of porous Si, and the oxygen ion implantation method.

[0009]

In the FIPOS method, an n-type Si layer is formed on a surface of a p-type Si single-crystal substrate in the island shape through the proton ion implantation (Imai et al., J. Crystal Growth, vol 63, 547 (1983))

or through the epitaxial growth and the patterning, then only the p-type Si substrate is rendered porous so as to surround the Si island from the surface by means of the anodizing method in a HF solution, and thereafter the n-type Si island is dielectric-isolated through accelerating oxidation. In this method, there is a problem that the isolated Si region is determined in advance of the device process so that the degree of freedom of device designing is limited.

[0010]

The oxygen ion implantation method is a method called SIMOX first reported by K. Izumi. After implanting about 10^{17} to $10^{18}/cm^2$ of oxygen ions into an Si wafer, the ion-implanted Si wafer is annealed at the high temperature of about 1,320°C in the atmosphere of argon/oxygen. As a result, oxygen ions implanted with respect to a depth corresponding to a projection range (Rp) of ion implantation are bonded with silicon so as to form a silicon oxide layer. On this occasion, a silicon layer which has been rendered amorphous at an upper portion of the silicon oxide layer due to the oxygen ion implantation is also recrystallized so as to be a single-crystal silicon layer. Conventionally, there have been a lot of defects included in the silicon layer on the surface, that is, about $10^5/cm^2$. On the other hand, by setting an implantation amount of oxygen to about $4\times10^{17}/cm^2$, defects are successfully reduced to about

$10^2/cm^2$. However, since the ranges of implantation energy and implantation amount for maintaining the quality of the silicon oxide layer, the crystalline property of the surface silicon layer and the like are so narrow that thicknesses of the surface silicon layer and the buried silicon oxide (BOX: buried oxide) layer were limited to particular values. For achieving a desired thickness of the surface silicon layer, it was necessary to perform sacrificial oxidation and epitaxial growth. In this case, there is a problem that, since the degradation caused through these processes is superposed on the distribution of thicknesses, the thickness uniformity is deteriorated.

[0011]

It has been reported that a formation failure region of silicon oxide called a pipe exists in the BOX layer. As one cause of this, the foreign matter upon implantation, such as dust, is considered. In the portion where the pipe exists, the deterioration of the device characteristic is generated due to leak between an active layer and a support substrate.

[0012]

Further, since the ion implantation in the SIMOX is large in implantation amount as compared with the ion implantation in the ordinary semiconductor process as mentioned above, implantation time is long even after the apparatus to be used exclusively for that matter has been

developed, which implantation time might be of the order of hour. The ion implantation is performed by raster-scanning an ion beam of a given current amount or expanding the beam so that increment of the implantation time is predicted following increment in area of the wafer. Further, in the high temperature heat treatment of the large-area wafer, it has been pointed out that a problem of occurrence of slip due to the temperature distribution in the wafer becomes severer. In the SIMOX, the heat treatment is essential at the high temperature, that is, 1,320°C, which is not normally used in the silicon semiconductor process, so that there has been concern that this problem including the development of the apparatus becomes more significant.

[0013]

On the other hand, apart from the foregoing conventional SOI forming method, attention has been recently given to the method which forms the SOI structure by sticking an Si single-crystal substrate to a thermal-oxidized Si single-crystal substrate through the heat treatment or using adhesives. In this method, it is necessary to form an active layer for the device into a uniform thin film. Specifically, it is necessary to form an Si single-crystal substrate of a thickness of as much as hundreds of microns into a film of several microns or less. There are two kinds of methods for thickness reduction as follows:

[0014]

1. Thickness reduction through polishing;
2. Thickness reduction through local plasma etching;
3. Thickness reduction through selective etching.

[0015]

In the polishing of 1, the uniform thickness reduction is difficult. Particularly, in case of thickness reduction to submicrons, the irregularity amounts to as much as tens of percents so that uniformalization is a big problem. If the size of wafer is further enlarged, the difficulty is increased correspondingly.

[0016]

In the method of 2, after reducing the thickness to about 1 to 3μm through the polishing of 1, the thickness distribution is measured at many points. Thereafter, by scanning the plasma using the SF6 of a diameter of several millimeters based on the thickness distribution, etching is performed while correcting the thickness distribution, so as to reduce the thickness to a given value. In this method, it has been reported that the thickness distribution can be within the range of about ±10nm. However, if the foreign matter (particles) exists on the substrate upon plasma etching, the foreign matter works as an etching mask so that projections are formed on the substrate.

Since the surface is rough immediately after the

etching, touch polishing is necessary after completion of the plasma etching. The polishing amount is controlled based on the time management, and hence, the final film thickness control and the deterioration of film thickness distribution due to polishing have been pointed out. Further, in the polishing, abrasives such as colloidal silica directly rub the surface working as an active layer so that there has been concern about formation of a fracture layer due to polishing and introduction of processing distortion. Further, if the wafer is increased in area to a large extent, since the plasma etching time is increased in proportion to increment of the wafer area, there is concern about extreme reduction of the throughput.

[0017]

In the method of 3, a film structure capable of selective etching is formed in advance in a substrate to be formed into a film. For example, a p^+-Si thin layer containing boron in the concentration no less than $10^{19}/cm^3$ and a p^--Si thin layer are formed on a p^- substrate using the method of, for example, the epitaxial growth so as to form a first substrate. The first substrate is bonded with a second substrate via an insulating layer such as an oxide film, and then the underside of the first substrate is ground or polished in advance so as to reduce in thickness. Thereafter, the p^+ layer is exposed through the selective etching of the p^-

layer and further the p^- layer is exposed through the selective etching of the p^+ layer, so as to achieve the SOI structure. This method is detailed in the report of Maszara.

Although the selective etching is said to be effective for uniform thickness reduction, it has the following problems:

The ratio of etching selectively is 10^2 at most, which is not sufficient.

Since the surface property after etching is bad, the touch polishing is required after etching. However, as the result thereof, the film thickness is reduced and the thickness uniformity tends to be deteriorated. Particularly, although the polish amount is managed based on time, since dispersion of the polish speed is large, the control of the polish amount is difficult. Thus, it becomes a problem particularly in forming an extremely thin SOI layer of, for example, 100nm.

The crystalline of the SOI layer is bad because of using the ion implantation, the epitaxial growth or the heteroepitaxial growth on the high-concentration B dope Si layer.

The surface property of a surface to be bonded with is inferior to the normal silicon wafer (C. Harendt, et. al., J. Elect. Mater. Vol. 20, 267 (1991), H. Baumgart, et. al., Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-733 (1991), C.E. Hunt,

Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-696 (1991)). Further, the selectivity of selective etching largely depends a difference in concentration of impurities such as boron and sharpness of the profile in the depth direction. Accordingly, if the high-temperature bonding annealing for increasing the bonding strength or the high-temperature epitaxial growth for improving the crystallinity is performed, the depth direction distribution of the impurity concentration expands so that the selectivity of etching is deteriorated. That is, it is difficult to improve both the ratio of etching selectivity and the crystallinity or the bonding strength.

[0018]

[Problems to be solved by the Invention]

Recently, in view of the foregoing problems, Yonehara and collaborators have reported the bonded SOI which is excellent in thickness uniformity and crystalline property and capable of batch processing. Brief explanation about this will be given using in Fig. 6. In this method, a porous layer 62 formed on an Si substrate 61 is used as a material for selective etching ((a) in Fig. 6). After epitaxial-growing a non-porous single-crystal Si layer 63 on the porous layer 62 ((b) in Fig. 6), the three-layer composite is bonded with a support substrate 64 via the oxidized Si layer 63 ((c) in Fig. 6). The Si substrate

61 is reduced in thickness through grinding or the like from the underside so as to expose the porous Si 62 all over the substrate ((d) in Fig. 6). The exposed porous Si 62 is removed through etching using a selective etching liquid, such as, KOH or $HF+H_2O_2$ ((d) in Fig. 6). At this time, since the ratio of etching selectively of porous Si relative to bulk Si (non-porous single-crystal silicon) can be set fully high, that is, 100,000 times, the non-porous single-crystal silicon layer grown on the porous layer in advance can be left on the support substrate without being hardly reduced in thickness, so as to form the SOI substrate. Accordingly, the thickness uniformity of the SOI is substantially determined during the epitaxial growth. Since a CVD apparatus used in the normal semiconductor process can be used for the epitaxial growth, according to the report of Sato and collaborator, the thickness uniformity is realized, for example, within 100nm ± 2%. Further, the crystallinity of the epitaxial silicon layer is also excellent and has been reported to be $3.5\times10^2/cm^2$.

[0019]

In the conventional method, since the selectivity of etching depends on the difference in impurity concentration and the depth direction profile, the temperature of the heat treatment (bonding, epitaxial growth, oxidation or the like) which expands the concentration distribution is largely limited to

approximately no higher than 800°C. On the other hand, in the etching of this method, since the difference in structure between porous and bulk determines the etching speed, the limitation of the heat treatment temperature is small. It has been reported that the heat treatment at about 1,180°C is possible. For example, it is known that the heat treatment after bonding enhances the bonding strength between the wafers and reduces the number and size of voids generated at the bonded interface. Further, in the etching based on such a structural difference, the particles, even if adhered on porous silicon, do not affect the thickness uniformity.

[0020]

On the other hand, in general, on a light transmittable substrate, typically glass, the deposited thin Si layer only becomes amorphous or polycrystalline at best, reflecting disorderliness in crystal structure of the substrate, so that the high-performance device can not be produced. This is due to the crystal structure of the substrate being amorphous, and thus an excellent single-crystal layer can not be achieved even by merely depositing the Si layer.

[0021]

However, the semiconductor substrate obtained through bonding normally requires two wafers one of which is removed wastefully for the most part through polishing, etching or the like, so that the finite

resources of the earth are wasted.

[0022]

Accordingly, in the conventional method, the bonded SOI has various problems about controllability, uniformity and economics.

[0023]

A method is proposed in Japanese Patent Application No. 7-045441 for recycling the first substrate which is wasted in such a bonding method.

[0024]

In this method, the following method is adopted, in the foregoing bonding and etch-back method using the porous Si, instead of the step for reducing in thickness the first substrate through grinding, etching or the like from the underside so as to expose the porous Si. This will be explained using in Fig. 7.

[0025]

After forming porous a surface layer 72 of by making the surface layer of a first Si substrate 71 porous ((a) in Fig. 7), a single-crystal Si layer 73 is formed thereon ((b) in Fig. 7). Then, the single-crystal Si layer along with the Si substrate is bonded to a main surface of a second Si substrate 74 which is different from the first Si substate, working as a support substrate, via an insulating layer therebetween ((c)in Fig. 7). Thereafter, the bonded wafers are separated at the porous layer and the porous Si layer exposed on the surface at the side of the second Si

substrate is selectively removed so that the SOI substrate is formed. Separation of the bonded wafers is performed, for example, a method selected from the following methods that the tensile force or pressure is sufficiently applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane; that the wave energy such as the ultrasonic wave is applied; that the porous layer is exposed at the wafer end surfaces, the porous Si is etched to some extent, what is like a razor blade is inserted thereinto; that the porous layer is exposed at the wafer end surfaces and a liquid such as water is impregnated into the porous Si, and the whole bonded wafers are heated or cooled to expand the liquid; and that the force is applied to the first (or the second) substrate in parallel to the second (or the first) substrate.

[0026]

Each of these methods is based on the fact that, although the mechanical strength of the porous Si layer 72 differs depending on the porosity, it is considered to be much weaker than the bulk Si. For example, if the porosity is 50%, the mechanical strength can be considered to be half the bulk. Specifically, when a compressive, tensile or shear force is applied to the bonded wafers, the porous Si layer is first ruptured. As the porosity is increased, the porous layer can be

ruptured with a weaker force.

[0027]

However, if the porosity of porous silicon is increased, it is possible that distortion is introduced due to the ratio of bulk silicon relative to the lattice constant being increased so as to increase warpage of the wafer. As a result, the following problems may be raised, that is, the number of void bonding failure regions called void is increased upon bonding, the crystal defect density is increased and, in the worst case, cracks are introduced into the epitaxial layer, and slip lines are introduced on the periphery of the wafer due to influence of thermal distortion upon the epitaxial growth.

[0028]

When applying the force in the vertical or horizontal direction relative to the surface of the wafer, since the semiconductor substrate is not a fully rigid body but an elastic body, the wafer may be subjected to elastic deformation depending on a supporting fashion of the wafer so that the force escapes and thus is not applied to the porous layer effectively. Similarly, when inserting what is like a razor blade from the wafer end surface, unless the razor blade is fully thin and fully high in rigidity, the yield may be lowered.

[0029]

Further, if the bonding strength at the bonded interface is weaker as compared with the strength of the porous Si layer or if weak portions exist locally, the two wafers may be separated at the bonded interface so that the initial object can not be achieved.

[0030]

Further, since, in any of the methods, the position where separation occurs in the porous layer is not fixed, if the ratio in etching speed between the porous Si and the bulk Si is not sufficient, the epitaxial silicon layer is first etched more or less at a portion where the porous layer remains thin rather than at a portion where the porous layer remains thick. Thus, the thickness uniformity of the SOI layer may be deteriorated. Particularly, when the final thickness of the SOI layer is reduced to about 100nm, the thickness uniformity is deteriorated so that a problem may be raised when forming the element such as the fully depleted MOSFET whose threshold voltage is sensitive to the film thickness.

[0031]

In view of the foregoing, the method has been demanded for producing, with high reproducibility, the SOI substrate which is high in quality and simultaneously for achieving resources saving and reduction in cost through recycling of the wafer.

[0032]

On the other hand, in general, on a light

transmittable substrate, typically glass, the deposited thin Si layer only becomes amorphous or polycrystalline at best, reflecting disorderliness in crystal structure of the substrate, so that the high-performance device can not be produced. This is due to the crystal structure of the substrate being amorphous, and thus an excellent single-crystal layer can not be achieved even by merely depositing the Si layer.

[0033]

The light transmissible substrate is important for constituting a contact sensor as being a light-receiving element or a projection-type liquid-crystal image display device. For achieving further densification, further high resolution and further fineness of pixels (picture elements) of the sensor or the display device, the high-performance drive element is required. As a result, it is necessary to produce the element on the light transmissible substrate using the single-crystal layer having the excellent crystallinity.

[0034]

Further, when using the single-crystal layer, reduction in size and acceleration of a chip can be achieved by incorporating a peripheral circuit for driving the pixels and an image processing circuit into the same substrate having the pixels.

[0035]

Specifically, in case of amorphous Si or

polycrystalline Si, it is difficult, due to its defective crystal structure, to produce the drive element having the performance which is required or will be required in the future.

[0036]

On the other hand, for producing the device of the compound semiconductor, the substrate of the compound semiconductor is essential. However, the compound semiconductor substrate is expensive and further is very difficult to be increased in area to a large extent.

[0037]

Further, an attempt has been made to achieve the epitaxial growth of the compound semiconductor such as GaAs on the Si substrate. However, due to difference in lattice constant or thermal expansion coefficient, the grown film is poor in crystallinity and thus is very difficult to be applied to the device.

[0038]

Further, an attempt has been made to achieve the epitaxial growth of the compound semiconductor on porous Si for reducing misfit of lattice. However, due to low thermostability and aged deterioration of porous Si, the stability and the reliability are poor as the substrate during or after production of the device. However, there is a problem that the compound semiconductor substrate is expensive and low in mechanical strength so that the large-area wafer is difficult to be produced.

[0039]

In view of the foregoing, an attempt has been made to achieve the heteroepitaxial growth of the compound semiconductor on the Si wafer which is inexpensive and high in mechanical strength so that the large-area wafer can be produced.

[0040]

Further, recently, attention has been given to porous silicon also as a luminescent material for photoluminescence, electroluminescence or the like, and many research reports have been made therefor. In general, the structure of porous silicon largely differs depending on the type (p, n) and the concentration of impurities contained in silicon. When the p-type impurities are doped, the structure of porous silicon is roughly divided into two kinds depending on whether the impurity concentration is no less than $10^{18}/cm^3$ or no more than $10^{17}/cm^3$. In the former case, the pore walls are relatively thick, that is, from several nanometers to several tens of nanometers, the pore density is about $10^{11}/cm^2$ and the porosity is relatively low. However, it is difficult for this porous silicon to serve for luminescence. On the other hand, in the latter case, as compared with the former case, porous silicon whose pore wall is no more than several nanometers in thickness, whose pore density is greater by one figure and whose porosity exceeds 50%, can be easily formed. Most of

luminous phenomena, such as photoluminescence, are mainly based on the formation of porous silicon using the latter as a starting material. However, the mechanical strength is low corresponding to the largeness of porosity. Further, since a lattice constant deviation relative to bulk Si is as much as 10^{-3} (about 10^{-4} in the former case), there has been a problem that, when epitaxial-growing the single-crystal silicon layer on such porous silicon, defects are largely introduced into the epitaxial Si layer and cracks are further introduced thereinto. On the other hand, for utilizing the fine porous structure, which is suitable for a luminescent material, as a light-emitting device, it has been desired that the epitaxial Si layer be formed on porous silicon for providing a contact or the MOSFET or the like as a peripheral circuit be formed on the epitaxial silicon layer.

[0041]

[Means for solving the Problems]

The present invention has an object to provide a semiconductor substrate and a forming method thereof which can solve the foregoing various problems by superposing a finer porous structure in a porous layer.

[0042]

A first embodiment of a semiconductor substrate according to the present invention is characterized by a semiconductor substrate comprising a porous Si layer as a surface layer of at least one main plane side of an Si

substrate and a porous Si layer having a thin pore wall included in said porous Si layer.

[0043]

A first embodiment of a process for preparing a semiconductor substrate according to the present invention is characterized by a process for preparing a semiconductor substrate comprising the steps of rendering the surface layer of at least one main plane side of an Si substrate porous, and ion implanting at least one element of rare gases, hydrogen and nitrogen into the porous Si layer with a given projection range.

[0044]

According to the first embodiment of the present invention, for example, a structure can be easily achieved, wherein a porous layer having a fine structure to work as a luminescent material is sandwiched in a porous layer having a high mechanical strength, such as porous silicon formed on a p^+-Si substrate. Although the porous layer having such a fine structure differs from bulk Si in lattice constant, by sandwiching it in the large porous Si layer having intermediate lattice constant, stresses can be relaxed and introduction of cracks or defects can be suppressed. Specifically, since the luminescent layer which is stable in structure can be formed, it is not only possible to serve for formation of peripheral circuit or wiring, but also possible to provide a material which is excellent in long-term

stability.

[0045]

A second embodiment of a semiconductor substrate according to the present invention is characterized by a semiconductor substrate totally comprising porous Si in a thickness direction and having a total film thickness of 20 μm or less. A second embodiment of a process for preparing a semiconductor substrate according to the present invention is characterized by comprising the steps of rendering the surface layer of at least one main plane side of a first Si substrate porous, ion implanting at least one element of rare gases, hydrogen and nitrogen with a projection range in said porous layer, and separating the semiconductor substrate into two in said porous Si.

[0046]

According to the second embodiment of the present invention, an extremely thin porous layer corresponding to a projection range of ion implantation can be formed. Since the pore size of such a porous layer can be set small, that is, no greater than several tens of nanometers, even the small foreign matter contained in gas and exceeding several tens of nanometers in diameter can be removed. Further, a thickness of such a porous layer can be set small, that is, no greater than 20μm, the conductance of the gas can be ensured. Specifically, when using it as a filter for particles in the gas, it is

possible to produce a filter which can remove the particles greater than several tens of nanometers in diameter and whose pressure loss is small. Further, if high purity Si which is used in the semiconductor process is used as a substrate, there is no worry about contamination from the filter itself. Further, according to the second embodiment of the present invention, after separation of the porous substrate, the first Si substrate can be reused. Also, the first Si substrate can repeatedly be reused until it can not be used relating to its strength.

[0047]

A third embodiment of a semiconductor substrate of the present invention is characterized by a semiconductor substrate comprising a non-porous thin film on a porous Si layer of at least one main plane side of a semiconductor substrate and a porous layer having a pore wall thinner than that of other porous portion included in said porous Si layer.

[0048]

A third embodiment of a process for preparing a semiconductor substrate according to the present invention characterized by comprising the steps of rendering the surface of at least one main plane side of a first Si substrate porous, forming a non-porous thin film on said porous Si layer, and ion implanting at least one element of rare gases, hydrogen and nitrogen into

said porous Si layer with a given projection range.

[0049]

According to the third embodiment of the present invention, since a porous layer with a fine structure can be formed after forming a single-crystal silicon layer on a porous layer, eptaxial growth conditions of a single-crystal layer can be set without being influenced by a structural change of the porous layer etc. Namely, the porous layer with a fine structure as a luminescent layer with tends to change by heat-treatment and the like after completion of the heat-treatment for film formation so that the element characteristics do not change by after-treatment such as heat treatment.

[0050]

A fourth embodiment of a process for preparing a semiconductor substrate according to the present invention is characterized by comprising the steps of bonding the main plane of a first Si substrate having a non-porous thin film formed on a porous Si layer to the main plane of a separately prepared second substrate, separating the bonded substrate at the porous Si layer, and selectively removing the porous layer exposed on the surface of the second substrate.

[0051]

Further, a process for preparing a semiconductor substrate according to the present invention includes the following embodiment.

[0052]

Specifically, an embodiment is characterized by a process for preparing a semiconductor substrate comprising the steps of rendering the surface layer of a main plane side of a first Si substrate porous, forming a non-porous layer on said porous Si layer, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layer with a given projection range, bonding the main plane of said first Si substrate to a main plane of second substrate, separating the bonded substrate at said porous Si layer, and selectively removing the porous layer exposed on the surface of the second substrate.

[0053]

Another embodiment is characterized by a process for preparing a semiconductor substrate comprising the steps of rendering the surface layer of a main plane side of a first Si substrate porous, forming a non-porous layer on said porous Si layer, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layer with a given projection range, bonding said first Si substrate to a main plane of a second substrate, separating the bonded substrate at said porous Si layer, selectively removing the porous Si layer exposed on the surface of the second substrate, again forming a non-porous layer on the porous silicon layer exposed on the surface of the first substrate, and ion implanting at

least one element of rare gases, hydrogen and nitrogen into said porous layer with a given projection range.

[0054]

Further embodiments characterized by a process for preparing a semiconductor substrate comprising the steps of rendering the surface layers located at two main plane sides of a first Si substrate porous, forming a non-porous layer on each of said porous Si layers of the two main planes, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layers of said two main planes with a given projection range, bonding each of the two main planes respectively to each main plane of separately prepared two support substrates, separating the bonded substrate into three at said porous Si layers, and selectively removing said porous Si layer exposed on the surfaces of said two support substrate.

[0055]

Further embodiment is characterized by a process for preparing a semiconductor substrate comprising the steps of rendering the surface layers located at two main sides of a first Si substrate porous, forming a non-porous layer on each of said porous Si layers of the two main planes, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layers of said two main planes with a given projection range, bonding each of the two main planes respectively to each main plane of separately prepared two support substrate,

separating the bond wafer into three at said porous Si layers, selectively removing said porous Si layer exposed on the surfaces of said two support substrate, and removing said porous Si layer remained on the first substrate.

[0056]

Further embodiment is characterized by a process for preparing a semiconductor substrate comprising the steps of rendering the surface layer located at two main plane sides of a first Si substrate porous, forming a non-porous layer on each of said porous Si layers of the two main planes, ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layers of said two main planes with a given projection range, bonding each of the two main planes respectively to each main plane of separately prepared two support substrate, separating the bonded wafer into three at said porous Si layers, selectively removing said porous Si layer exposed on the surfaces of said two support substrate, again forming a non-porous layer on the porous silicon layer exposed on the surface of the first Si substrate, and ion implanting at least one element of rare gases, hydrogen and nitrogen into said porous layer with a given projection range.

[0057]

After removing the remaining porous layer, the first Si substrate separated by the foregoing method may be

reused as a first Si substrate by performing the surface flattening process if the surface flatness property is insufficient. The surface flattening process may be polishing, etching or the like normally used in the semiconductor process. On the other hand, the heat treatment in the atmosphere including hydrogen may also be used. By selecting the condition, this heat treatment can achieve the flatness to an extent where the atomic step is locally presented.

[0058]

According to the producing method of the semiconductor substrate of the present invention, upon removal of the first Si substrate, the Si substrate can be separated at one time in large area via the porous layer. Thus, the process can be shortened. Further, since the separating position is limited to within the porous layer with large porosity due to the ion implantation, thicknesses of the porous layer remaining on the second substrate side can be uniform so that the porous layer can be removed with excellent selectivity.

[0059]

According to the present invention, by previously ion implanting at least one element of rare gases, hydrogen and nitrogen into the porous layer with a given projection range, the Si substrate can be separated in advance at one time in large area via the porous layer. Thus, the grinding, polishing or etching process which

was essential in the prior art for removing the Si substrate to expose the porous silicon layer can be omitted to shorten the process. Further, since the separating position is limited to within the porous layer with large porosity by implanting ions of at least one kind of noble gas, hydrogen and nitrogen into the porous layer so as to have the projection range, thicknesses of the porous layer remaining on the second substrate side can be uniform so that the porous layer can be removed with excellent selectivity. Namely, the grinding or etching process which was essential in the prior art for exposing the porous silicon can not only be omitted, but also the separated first Si substrate can be reused as a first Si substrate by removing the remaining porous layer. If the surface flatness is insufficient in the Si substrate after removing the porous layer, a surface flattening treatment is performed. Since the separation site of the bonded two substrates is determined by the projection range, the separation site does not disperse different from the prior art. Therefore, upon removal of the porous silicon, it does not happen that the earlier exposed single-crystal silicon layer is etched to deteriorate the film thickness uniformity. Further, the first Si substrate can be repeatedly be reused until it not be used relating to it strength. Further, since the separation site of the substrate is limited to near the depth corresponding the projection range of ion

implantation, the thickness of the porous layer can be thin compared with that of the prior art.

[0060]

Alternatively, without removing the remaining porous layer, the separated first Si substrate can be reused again as a first Si substrate of the present invention by forming a non-porous single-crystal Si layer. Also in this case, the first Si substrate can be reused in the desired number of times until its structural strength makes it impossible.

[0061]

In the conventional method of producing the bonded substrates, the first Si substrate is gradually removed from one side thereof through grinding or etching. Thus, it is impossible to effectively use both sides of the first Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the first Si substrate is held in the initial state other than its surface layers so that, by using both sides of the first Si substrate as the main surfaces and bonding the support substrates to the sides of the first Si substrate, respectively, two bonded substrates can be simultaneously produced from one first Si substrate. Thus, the process can be shortened and the productivity can be improved. As appreciated, also in this case, the separated first Si substrate can be recycled as an Si substrate after removing the remaining porous Si.

[0062]

Specifically, the present invention uses a single-crystal Si substrate which is excellent in economics, flat and uniform over a large area and has an extremely excellent crystallinity, and removes from one side thereof to an Si or compound semiconductor active layer formed on the surface which thus remains, so as to provide a single-crystal Si layer or a compound semiconductor single-crystal layer with extremely less defects on an insulating material.

[0063]

The present invention provides a producing method of a semiconductor substrate which is capable of achieving an Si or compound semiconductor single-crystal layer with a crystallinity as good as a single-crystal wafer on a transparent substrate (light transmittable substrate), with high productivity, high uniformity, excellent controllability and reduced cost.

[0064]

Further, the present invention provides a producing method of a semiconductor substrate which is replaceable for an expensive SOS or SIMOX upon producing a large scale integrated circuit of an SOI structure.

[0065]

According to the present invention, the single-crystal compound semiconductor layer with excellent crystallinity can be formed on porous Si, and further,

this semiconductor layer can be transferred onto the large-area insulating substrate which is excellent in economics. Thus, the foregoing problem of the difference in lattice constant and thermal expansion coefficient can be sufficiently suppressed so as to form the compound semiconductor layer with excellent crystallinity on the insulating substrate.

[0066]

Further, since porous Si has a low mechanical strength and an extensive surface area, removal of the porous Si layer of the present invention can also be performed by selective polishing using the single-crystal layer as a polishing stopper.

[0067]

[Embodiments of the Present Invention]

The present invention simultaneously solves the foregoing various problems by superposing a finer porous structure in the foregoing porous layer.

[0068]

It has been reported that, by performing ion implantation of helium or hydrogen into bulk silicon and applying heat thereto, micro-cavities having diameters in the range from several nanometers to several tons of nanometers are formed at the implanted region in the density of as much as 10^{16} to $10^{17}/cm^3$ (for example, A. Van Veen, C.C. Griffioen, and J. H. Evans, Mat. Res. Soc. Symp. Proc. 107 (1988, Material Res. Soc. Pittsburgh,

Pennsylvania) p. 449). Recently, it has been researched to utilize these micro-cavity groups as gettering sites of metal impurities.

[0069]

V. Raineri and S.U. Campisano implanted helium ions into bulk silicon and applied a heat treatment thereto so as to form the cavity groups, then exposed the sides of the cavity groups by forming grooves in the substrate and applied an oxidation treatment thereto. As a result, the cavity groups were selectively oxidized so as to form a buried silicon oxide layer. That is, they reported that the SOI structure could be formed (V. Raineri and S.U. Campisano, Appl. Phys. Lett. 66 (1995) p. 3654). However, in their method, thicknesses of the surface silicon layer and the buried silicon oxide layer were so limited as to achieve both formation of the cavity groups and relaxation of stresses introduced due to volume expansion upon oxidation and further the formation of the grooves were necessary for selective oxidation so that the SOI structure could not be formed all over the substrate. Such formation of the cavity groups have been reported as a phenomenon following the implantation of light elements into metal along with an expansion or separation phenomenon of the cavity groups as a part of the research about a first reactor wall of the nuclear fusion reactor.

[0070]

Porous Si was found in the course of the research of electropolishing of the semiconductor in 1956 by Uhlir and collaborator (A. Uhlir, Bell Syst. Tech. J., vol. 35, 333 (1956)). Porous silicon can be formed by anodizing the Si substrate in the HF solution. Unagami and collaborator researched the dissolution reaction of Si in the anodization and reported that positive holes were necessary for the anodizing reaction of Si in the HF solution and the reaction was as follows (T. Unagami, J. Electrochem. Soc., vol. 127, 476 (1980)):

[0071]

$$Si + 2HF + (2-n)\ e^{+} \rightarrow SiF_2 + 2H^{+} + ne^{-}$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

or

$$Si + 4HF + (4-\lambda)\ e^{+} \rightarrow SiF_4 + 4H^{+} + \lambda e^{-}$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

wherein e^{+} and e^{-} represent a hole and an electron, respectively, and n and λ represent the numbers of holes necessary for dissolution of one Si element, respectively. It was reported that porous Si was formed when $n>2$ or $\lambda>4$ was satisfied.

[0072]

As appreciated from the foregoing, p-type Si having the holes is rendered porous while n-type Si is not rendered porous. The selectivity while getting porous has been proved by Nagano and collaborators and Imai

(Nagano, Nakajima, Yasuno, Oonaka, Kajiwara, Engineering Research Report of Institute of Electronics and Communication Engineers of Japan, vol. 79, SSD79-9549 (1979)), (K. Imai, Solid-State Electronics, vol. 24, 159 (1981)).

[0073]

However, there have also been reports that high-concentration n-type Si can be rendered porous (R.P. Holmstrom and J.Y. Chi, Appl. Phys. Lett., vol. 42, 386 (1983)) so that it is important to choose the substrate which can be rendered porous, irrespective of p- or n-type.

[0074]

Porous silicon can be formed by anodizing the Si substrate in the HF solution. The porous layer has a structure like sponge including holes of about 10^{-1} to 10nm in diameter arranged at intervals of about 10^{-1} to 10nm. The density thereof can be changed in the range of 1.1 to 0.6g/cm^3 by changing the HF solution concentration in the range of 50 to 20% and by changing the current density, as compared with the density 2.33g/cm^3 of the single-crystal Si. That is, the porosity can be changed. Although the density of porous Si is no more than half as compared with the single-crystal Si as described above, the monocrystalline property is maintained so that the single-crystal Si layer can be epitaxial-grown at the upper part of the porous layer. However, at the

temperature no less than 1,000°C, rearrangement of the internal holes occurs to spoil the accelerating etching characteristic. In view of this, it has been said that the low temperature growth, such as the molecular beam epitaxial growth, the plasma CVD, the vacuum CVD, the optical CVD, the bias sputtering or the liquid deposition, is suitable for the epitaxial growth of the Si layer. On the other hand, if a protective film is formed in advance on the pore walls of the porous layer by means of the method of low temperature oxidation or the like, the high temperature growth is also possible.

[0075]

Further, the porous layer is reduced in density to no more than half due to the formation of a lot of the internal cavities therein. As a result, since the surface area is greatly increased as compared with the volume, the chemical etching speed thereof is extremely increased as compared with the etching speed of the normal single-crystal layer.

[0076]

Although the mechanical strength of porous Si differs depending on porosity, it is considered to be smaller than that of bulk Si. For example, if porosity is 50%, the mechanical strength can be considered to be half the bulk. Specifically, when a compressive, tensile or shear force is applied to the bonded wafers, the porous Si layer is first ruptured. As the porosity is

increased, the porous layer can be ruptured with a weaker force.

[0077]

The present invention simultaneously solves the foregoing various problems by superposing a finer porous structure in the foregoing porous layer at the region of a constant depth from the surface of the porous layer.

[0078]

It has been found that, when ion implantation of at least one kind of rare gases, hydrogen and nitrogen is performed into the porous layer with a projection range ensured, the porosity of the implanted region is increased. When observing in detail the implanted layer using an electron microscope, a lot of micro-cavities were formed in the pore walls of the porous layer formed in advance. Specifically, the fine porous structure was formed. Upon irradiation of ultraviolet light, the luminous phenomenon at the wavelength around 700nm was confirmed.

[0079]

If choosing further implantation conditions, porous silicon can be separated at a depth corresponding to the projection range of the ion implantation.

[0080]

The separation can be improved in uniformity or achieved with less implantation amount by forming in advance a thin film on the pore walls of porous silicon

using the method of particularly low temperature oxidation. The separation can be facilitated by applying the heat treatment after the ion implantation.

[0081]

By ion-implanting at least one kind of noble gas, hydrogen and nitrogen into the porous layer with a projection range ensured after formation of at least one layer of non-porous thin film, such as a non-porous single-crystal silicon layer, on porous silicon or without such formation, the porosity of the implanted is increased. If such an Si substrate is bonded to the second substrate and then the bonded substrates are subjected to the mechanical force or the heat treatment, or even without such processes, the bonded two substrates can be separated into two at a portion of the porous silicon layer where ions are implanted.

[0082]

By supporting both sides of the ion-implanted layer with a fully thick elastic or rigid body, the separation can be achieved uniformly over the large area. Further, it is possible to facilitate the separation of the substrates by applying the heat treatment, the force or the ultrasonic wave to the substrates.

[0083]

Even if non-formation regions of the implanted layer are formed due to presence of the foreign matter on the surface upon the ion implantation, since the mechanical

strength of the porous layer itself is smaller than bulk Si, the separation occurs in the porous layer. Thus, the bonded two substrates can be separated without causing the cracks or the line in the non-porous single-crystal Si layer.

[0084]

Further, by selectively removing the porous Si layer remaining on the surface of the separated substrate using the method of etching, polishing or the like, the single-crystal Si layer can be transferred on the support substrate. On the other hand, after removing the remaining porous Si, the first Si substrate can be again formed with porous silicon, then formed with a single-crystal Si layer and subjected to the ion implantation of at least one kind of rare gases, hydrogen and nitrogen into the porous layer with the projection range ensured, and then bonded to a second substrate. That is, the first Si substrate can be recycled. Further, if the first Si substrate, with the porous silicon layer remaining, is subjected to the heat treatment in the reduction atmosphere including hydrogen or the like, the porous silicon surface is rendered flat and smooth so that the single-crystal silicon layer can be formed successively. By bonding the single-crystal silicon layer to the second substrate, the first Si substrate can also be recycled.

[0085]

According to this method, since the portion to be separated is limited to the ion-implanted region in the porous layer, the depth of the separated region is not dispersed in the porous layer. Thus, even if the ratio of etching selectivity of porous silicon is insufficient, porous silicon can be removed for substantially a constant time so that the uniformity of thickness of the single-crystal silicon layer provided on the second substrate is not spoiled.

[0086]

In the conventional method of producing the bonded substrates, the first Si substrate is gradually removed from one side thereof through grinding or etching. Thus, it is impossible to effectively use both sides of the first Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the first Si substrate is held in the initial state other than its surface layers so that, by using both sides of the first Si substrate as the main surfaces and bonding the support substrates to the sides of the first Si substrate, respectively, two bonded substrates can be simultaneously produced from one first Si substrate. As appreciated, also in this case, the first Si substrate can be recycled as a first Si substrate after removing the remaining porous Si.

[0087]

The second substrate may be, for example, a light

transmissible substrate, such as an Si substrate, an Si substrate with a silicon oxide film formed thereon, a silica glass substrate or a glass substrate, or a metal substrate, but not particularly limited thereto.

[0088]

The thin film formed on the porous Si layer on the first Si substrate may be, for example, a non-porous single-crystal Si film, a compound semiconductor film of such as GaAs or InP, a metal film or a carbon film, but not particularly limited thereto. Further, the thin film is not necessarily formed all over the porous Si layer, but may be partially etched by the patterning process.

[0089]

[Embodiment 1]

As shown in (a) of Fig. 1, an Si single-crystal substrate 11 is first prepared and then rendered porous 12 at its surface layer. As shown in (b) of Fig. 1, at least one kind of rare gases, hydrogen and nitrogen is ion-implanted into the porous layer. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{13}/cm^2$ and more preferably $1x10^{14}/cm^2$. When setting the projection

range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed according to necessity. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

[0090]

When the light of a mercury lamp, a xenon lamp or the like is applied to the thus produced sample as the light of shorter wavelength, the sample emits the red light around 780nm. That is, the photoluminescence is confirmed. Or an EL (Electroluminescence) element can be formed.

[0091]

In (b) of Fig. 1, the semiconductor substrate of the present invention is shown. The fine porous structure showing the luminous phenomenon is formed uniformly in large area all over the wafer. Further, the metallic luster is held on the surface, that is, not showing the stain manner as in the prior art, so that metallic wiring can be easily arranged.

[0092]

[Embodiment 2]

As shown in (a) of Fig. 2, an Si single-crystal substrate 21 is first prepared and then rendered porous 22 at its surface layer.

As shown in (b) of Fig. 2, at least one kind of rare gases, hydrogen and nitrogen is ion-implanted into the porous layer 22. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed or at least one of pressurization, tensile force and shearing stress is applied to the wafer in a direction perpendicular to the surface according to necessity, so as to divide the semiconductor substrate into two at the ion-implanted layer as a border. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

[0093]

In (c) of Fig. 2, the extremely thin porous substrate obtained by the present invention is shown. Since the division of the substrate starts spontaneously upon the heat treatment or the like as a trigger due to the internal stress introduced upon the implantation, the

extremely thin porous structure can be formed uniformly all over the substrate. The pores of the porous structure are formed from one main surface of the substrate toward the other main surface. Accordingly, when the gas is implanted under pressure from the one main surface, it is ejected out from the other main surface. In this case, since the pore size of the porous structure is in the range from several nanometers to several tens of nanometers, the particle greater than this can not pass therethrough. On the other hand, although the pressure loss is caused depending on the pore size, the pore density and a thickness of the extremely thin porous substrate, the strength of the substrate and the pressure loss can be both within the practical range if the thickness of the porous layer is approximately no more than 20μm.

[0094]

[Embodiment 3]

As shown in (a) of Fig. 3, an Si single-crystal substrate 31 is first prepared and then rendered porous 32 at its surface layer. Subsequently, as shown in (b) of Fig. 3, at least one layer is formed on the porous layer. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like.

[0095]

As shown in (c) of Fig. 3, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed according to necessity. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

[0096]

When the light of a mercury lamp, a xenon lamp or the like is applied to the thus produced sample as the light of shorter wavelength, the sample emits the red light around 780nm. That is, the photoluminescence is confirmed. Or an EL element can be formed.

[0097]

In (b) of Fig. 3, the semiconductor substrate of the present invention is shown. The fine porous structure

showing the luminous phenomenon is formed uniformly in large area all over the wafer. Further, the metallic luster is held on the surface, that is, not showing the cracks or the like as in the prior art, so that metallic wiring can be easily arranged.

[0098]

[Embodiment 4]

As shown in (a) of Fig. 4, an Si single-crystal substrate 41 is first prepared and then rendered porous at its surface layer. Numeral 42 denotes the obtained porous layer. Subsequently, as shown in (b) of Fig. 4, at least one non-porous thin film 43 is formed on the porous layer. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like. Or an element structure such as a MOSFET may be formed. As shown in (C) of Fig. 4, at least one kind of noble gas, hydrogen and nitrogen is ion-implanted into the porous layer 42 so as to form an implanted layer 44. When observing the implanted layer by a transmission electron microscope, formation of numberless micro-cavities can be seen. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation

amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed according to necessity. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

[0099]

As shown in (d) of Fig. 4, after abutting a second substrate 45 and the surface of the first substrate with each other at room temperature, they are bonded to each other through anodic bonding, pressurization, heat treatment or a combination thereof. As a result, both substrates are firmly coupled with each other.

[0100]

When single-crystal Si is deposited, it is preferable to perform the bonding after oxidized Si is formed on the surface of single-crystal Si through thermal oxidation or the like. On the other hand, the second substrate can be selected from among an Si substrate, an Si substrate with a silicon oxide film formed thereon, a light transmissible substrate such as quartz, a sapphire substrate and the like, but not

limited thereto as long as the surface serving for the bonding is fully flat. The bonding may be performed in three plies with an insulating thin plate interposed therebetween.

[0101]

Subsequently, the substrates are divided at the ion-implanted layer 44 in the porous Si layer 42 ((e) of Fig. 4). The structure of the second substrate side includes the porous Si layer 42, the non-porous thin film (for example, the single-crystal Si layer) 43 and the second substrate 45.

[0102]

Further, the porous Si layer 42 is selectively removed. In case of the non-porous thin film being single-crystal Si, only the porous Si layer 42 is subjected to the electroless wet chemical etching using at least one of the normal Si etching liquid, hydrofluoric acid being the porous Si selective etching liquid, a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to buffered hydrofluoric acid, so as to render the film formed in advance on the porous layer of the first substrate remain on the second substrate. As described above in detail, only the porous Si layer can be selectively etched using the normal Si etching liquid

due to the extensive surface area of porous Si. Alternatively, the porous Si layer 42 may be removed through selective polishing using the single-crystal Si layer 43 as a polishing stopper.

[0103]

In case of the compound semiconductor layer formed on the porous layer, only the porous Si layer 42 is subjected to chemical etching using the etching liquid which has the greater etching speed for Si relative to the compound semiconductor, so as to render the thickness-reduced single-crystal compound semiconductor layer 43 remain on the insulating substrates 44 and 45. Alternatively, the porous Si layer 42 is removed through selective polishing using the single-crystal compound semiconductor layer 43 as a polishing stopper.

[0104]

In (f) of Fig. 4, the semiconductor substrate of the present invention is shown. On the insulating substrates 15 and 14, the non-porous thin film, such as the single-crystal Si thin film 43, is formed in large area all over the wafer, flatly and uniformly reduced in thickness. The semiconductor substrate thus obtained can be suitably used also in view of production of the insulated electronic element.

[0105]

The first Si single-crystal substrate 41 can be reused as a first Si single-crystal substrate 41 after

removing remaining porous Si and after performing surface-flattening if the surface flat property is bad to an extent which is not admissible.

[0106]

Alternatively, a non-porous thin film may be again formed without removing porous Si so as to provide the substrate as shown in (b) of Fig. 4, which is then subjected to the processes shown in (c) to (f) of Fig. 4.

[0107]

[Embodiment 5]

As Shown in (a) of Fig. 5, a first Si single-crystal substrate 51 is first prepared and then rendered porous 52, 53 at both surface layers thereof. Subsequently, as shown in (b) of Fig. 5, at least one non-porous thin film 54, 55 is formed on each of the porous layers. The film to be formed is arbitrarily selected from among a single-crystal Si film, a polycrystalline Si film, an amorphous Si film, a metal film, a compound semiconductor film, a superconductive film and the like. Or an element structure such as a MOSFET may be formed.

[0108]

As shown in (c) of Fig. 5, at least one kind of rare gases, hydrogen and nitrogen is ion-implanted into the porous layers so as to form implanted layers 56 and 57. When observing the implanted layers by a

transmission electron microscope, formation of numberless micro-cavities can be seen, and accordingly the porosity enlarges. The charge condition of the implanted ions is not particularly limited. The acceleration energy is set such that the projection range corresponds to a depth at which the ion implantation is desired. Depending on the implantation amount, the size and the density of the micro-cavities to be formed are changed, but approximately no less than $1x10^{14}/cm^2$ and more preferably $1x10^{15}/cm^2$. When setting the projection range to be deeper, the channeling ion implantation may be employed. After the implantation, the heat treatment is performed according to necessity. In case of the heat treatment atmosphere being the oxidizing atmosphere, the pore walls are oxidized so that attention should be given to prevent the Si region from being all changed into silicon oxide due to overmuch oxidation.

[0109]

As shown in (d) of Fig. 5, after abutting two support substrates 58 and 59 and the surfaces of the non-porous thin films 54 and 55 of the first substrate with each other at room temperature, they are bonded to each other through anode bonding, pressurization, heat treatment or a combination thereof. As a result, the three substrates are firmly coupled with each other. Alternatively, the bonding may be performed in five plies with insulating thin plates interposed therebetween.

[0110]

When single-crystal Si is deposited, it is preferable to perform the bonding after oxidized Si is formed on the surface of single-crystal Si through thermal oxidation or the like. On the other hand, the support substrate can be selected from among an Si substrate, an Si substrate with a silicon oxide film formed thereon, a light transmissible substrate such as quartz, a sapphire substrate and the like, but not limited thereto as long as the surface serving for the bonding is fully flat.

[0111]

The bonding may be performed in three plies with an insulating thin plate interposed therebetween.

[0112]

Subsequently, the substrates are divided at the ion-implanted layers 56 and 57 in the porous Si layers 52 and 53 ((e) of Fig. 5). The structure of each of the two support substrate sides includes the porous Si layer 52, 53, the non-porous thin film (for example, the single-crystal Si layer) 54, 55 and the support substrate 58, 59.

[0113]

Further, the porous Si layer 52, 53 is selectively removed. In case of the non-porous thin film being single-crystal Si, only the porous Si layer 52, 53 is subjected to the electroless wet chemical etching using

at least one of the normal Si etching liquid, hydrofluoric acid being the porous Si selective etching liquid, a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to hydrofluoric acid, buffered hydrofluoric acid, and a mixed liquid obtained by adding at least one of alcohol and aqueous hydrogen peroxide to buffered hydrofluoric acid, so as to render the film formed in advance on the porous layer of the first substrate remain on the support substrate. As described above in detail, only the porous Si layer can be selectively etched using the normal Si etching liquid due to the extensive surface area of porous Si. Alternatively, the porous Si layer 52, 53 may be removed through selective polishing using the single-crystal Si layer 54, 55 as a polishing stopper.

[0114]

In case of the compound semiconductor layer formed on the porous layer, only the porous Si layer 52, 53 is subjected to chemical etching using the etching liquid which has the greater etching speed for Si relative to the compound semiconductor, so as to render the thickness-reduced single-crystal compound semiconductor layer 54, 55 remain on the insulating substrate. Alternatively, the porous Si layer 52, 53 is removed through selective polishing using the single-crystal compound semiconductor layer 54, 55 as a polishing stopper.

[0115]

In (f) of Fig. 5, the semiconductor substrates of the present invention are shown. On the support substrates, the non-porous thin films, such as the single-crystal Si thin films 54 and 55, are formed in large area all over the wafer, flatly and uniformly reduced in thickness, so that the two semiconductor substrates are simultaneously formed. The semiconductor substrates thus obtained can be suitably used also in view of production of the insulated electronic elements.

[0116]

The first Si single-crystal substrate 51 can be reused as a first Si single-crystal substrate 51 after removing remaining porous Si and after performing surface-flattening if the surface flat property is bad to an extent which is not admissible. Alternatively, a non-porous thin film may be again formed without removing porous Si so as to provide the substrate as shown in (b) of Fig. 5, which is then subjected to the processes shown in (c) to (f) of Fig. 5. The support substrates 58 and 59 are not necessarily identical with each other.

[0117]

[Examples]

Hereinbelow, the present invention will be described in detail using concrete examples. However, the present invention is not limited thereto.

[0118]

[Example 1]

A first p- or n-type (100) single-crystal Si substrate having 625μm in thickness, 0.01Ω∘cm in resistivity and 6 inches in diameter was anodized in an HF solution.

[0119]

The anodization condition was as follows:

[0120]

Current Density: 5 ($mA \circ cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0121]

Subsequently, helium ion, He^+ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the substrate at acceleration voltage of 30keV. Then, the substrate was subjected to the heat treatment at 850°C in the vacuum for 8 hours.

[0122]

When the light of a mercury lamp was applied to the substrate, luminescence of the red light with wavelength around 750nm was confirmed.

[0123]

[Example 2]

Two first p-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω∘cm in resistivity and 6 inches in diameter were prepared, and one of them

was anodized in an HF solution.

[0124]

The anodization condition was as follows:

[0125]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0126]

Helium ion, He^+ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 30keV. Subsequently, phosphorus ions of $5x10^{14}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 100keV. Then, these substrates were subjected to the heat treatment at 850°C in the vacuum for 8 hours. Further, ITO electrodes were vapor deposited on the surfaces.

[0127]

When the voltage was applied between the Si substrates and the ITO electrodes, luminescence of wavelength around 750nm was confirmed at the porous substrate, while luminescence was not confirmed at the other substrate.

[0128]

[Example 3]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter were prepared, and one of them was anodized in an HF solution.

[0129]

The anodization condition was as follows:

[0130]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 20 (μm)

Porosity: 15 (%)

[0131]

The anodized substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with a thermal-oxidized film. Subsequently, hydrogen ions of $1x10^{17}/cm^2$ were implanted all over the porous side of the porous substrate and all over the other substrate at acceleration voltage of 0.76MeV.

[0132]

When these substrates were subjected to the heat treatment at 1,000°C in the vacuum for 1 hour, the porous layer was separated uniformly all over the substrate with a thickness of about 1μm corresponding to the ion-implanted region, while a lot of swells like blisters

were only formed at the non-porous substrate.

[0133]

[Example 4]

A first p-type (100) single-crystal Si substrate having 625μm in thickness, 0.01Ω•cm in resistivity and 6 inches in diameter was anodized in an HF solution.

[0134]

The anodization condition was as follows:

[0135]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0136]

The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with a thermal-oxidized film. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.1μm on porous Si. The growing condition was as follows:

[0137]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900 °C

Growing Speed: 0.3 μm/min

[0138]

Helium ion, He^+ ions of $5x10^{16}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 30keV. Subsequently, phosphorus ions of $5x10^{14}/cm^2$ were implanted into the porous side of the anodized substrate and the surface side of the other substrate at acceleration voltage of 100keV. Then, these substrates were subjected to the heat treatment at 850°C in the argon atmosphere for 8 hours. Further, ITO electrodes were vapor deposited on the surfaces.

[0139]

When the voltage was applied between the Si substrate and the ITO electrode, luminescence of wavelength around 750nm was confirmed at the porous substrate.

[0140]

[Example 5]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω·cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

[0141]

The anodization condition was as follows:

[0142]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 3 (μm)

Porosity: 15 (%)

[0143]

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.15μm on porous Si. The growing condition was as follows:

[0144]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 950 °C

Growing Speed: 0.3 μm/min

[0145]

Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0146]

Subsequently, helium ion, He^+ ions of $1x10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 50keV.

[0147]

The surface of the SiO_2 layer and the surface of a

separately prepared support Si substrate formed with an SiO_2 layer of 500nm were overlapped and abutted with each other, and subjected to the heat treatment at 1,000°C for 2 hours so as to increase the bonding strength. Then, the two substrates were completely separated at a position corresponding to the projection range of the ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found. On the other hand, no change on the outward appearance was caused on the substrate which was not subjected to the helium ion implantation, and the substrates remained bonded to each other.

[0148]

Thus, the first Si substrate side of the bonded substrates (not subjected to the helium ion implantation) was ground using a grinder for the normal semiconductor so as to expose the porous Si layer. However, due to insufficient grinding accuracy, the whole porous layer could not be exposed.

[0149]

Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:5) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching

stopper and fully removed.

[0150]

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the ratio of etching selectivity relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0151]

Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. No change was caused on the single-crystal Si layer even by the selective etching of porous Si.

[0152]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0153]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0154]

[Example 6]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in

resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

[0155]

The anodization condition was as follows:

[0156]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0157]

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.15μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

[0158]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 950 °C

Growing Speed: 0.3 μm/min

[0159]

Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal

oxidation.

[0160]

Subsequently, hydrogen ions of $5x10^{16}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 50keV.

[0161]

The surface of the SiO_2 layer and the surface of a separately prepared support Si substrate formed with an SiO_2 layer of 500nm were overlapped and abutted with each other, and subjected to the heat treatment at 1,000°C for 2 hours so as to increase the bonding strength. Then, the two substrates were completely separated at a position corresponding to the projection range of the ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found. On the other hand, no change on the outward appearance was caused on the substrate which was not subjected to the hydrogen ion implantation, and the substrates remained bonded to each other.

[0162]

The first substrate side of the bonded substrates (not subjected to the hydrogen ion implantation) was ground using a grinder for the normal semiconductor so as to expose the porous layer. However, due to insufficient grinding accuracy, a thickness of the remaining porous layer was 1 to 9μm.

[0163]

Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

[0164]

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the ratio of etching selectivity relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0165]

Specifically, the single-crystal Si layer having 0.1μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 101nm ± 3nm with the hydrogen ion implantation, while it was 101nm ± 7nm without the hydrogen ion implantation so that it was confirmed that the thickness distribution was deteriorated due to influence of dispersion of thicknesses of porous silicon.

[0166]

Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0167]

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50μm square region was about 0.2nm which was equal to the silicon wafer on the market.

[0168]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0169]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0170]

At the same time, the porous Si layer remaining on the first Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed, and the Si substrate could be again put into the porosity-forming process.

[0171]

[Example 7]

Two first p- or n-type (100) single-crystal Si substrates each having 625μm in thickness, 0.01Ω•cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

[0172]

The anodization condition was as follows:

[0173]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH=1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0174]

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.55μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

[0175]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900 °C

Growing Speed: 0.3 μm/min

[0176]

Further, an SiO_2 layer of 100nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0177]

Subsequently, hydrogen ions of $5x10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100keV.

[0178]

The surface of the SiO_2 layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to increase the bonding strength. The sufficient pressure is applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane. Then, the porous Si layer was divided into two at the ion-implanted region.

[0179]

On the other hand, when the pressure was further applied to the substrate (not subjected to the helium ion implantation), the porous layer was ruptured into two. However, when observing the divided porous layers, cracks were introduced into portions of the single-crystal Si layer so that the substrate could not be put into the subsequent process.

[0180]

Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

[0181]

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0182]

Specifically, the single-crystal Si layer having 0.5 μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501 nm ± 11 nm with the hydrogen ion implantation. Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0183]

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness

at a 50 μm square region was about 0.2 nm which was equal to the silicon wafer on the market.

[0184]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0185]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer. Using the CVD (chemical vapor deposition) method, single-crystal Si was again epitaxial-grown by 0.55 μm on porous Si remaining at the first substrate side. The growing condition was as follows. The accuracy of the film thickness was ±2%.

[0186]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900°C

Growing Speed: 0.3 μm/min

[0187]

When evaluating the crystal defect density of this single-crystal Si layer through the defect revealing etching, the defect density was about $1 \times 10^3/cm^2$ and this substrate could be again put into the processes of ion implantation and bonding.

[0188]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0189]

[Example 8]

Two first p- or n-type (100) single-crystal Si substrates each having 625 μm in thickness, 0.01 Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

[0190]

The anodization condition was as follows:

[0191]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH$ = 1:1:1

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0192]

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.15 μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

[0193]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 950°C

Growing Speed: 0.3 μm/min

[0194]

Further, an SiO_2 layer of 100 nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0195]

Subsequently, helium ions of $1 \times 10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100 keV.

[0196]

The surface of the SiO_2 layer and the surface of a separately prepared support Si substrate formed with an SiO_2 layer of 500 nm were overlapped and abutted with each other, and subjected to the heat treatment at 400°C for 2 hours. The sufficient tensile force is applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane. Then, the two substrates were completely separated at a position corresponding to the projection range of the hydrogen ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found. On the other hand, when the pressure was further applied to the

substrate (not subjected to the helium ion implantation), the porous layer was ruptured into two. However, when observing the divided porous layers, cracks were introduced into portions of the single-crystal Si layer so that the substrate could not be put into the subsequent process.

[0197]

Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

[0198]

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0199]

Specifically, the single-crystal Si layer having 0.1 μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the

thicknesses was 101 nm ± 3 nm with the hydrogen ion implantation, while it was 101 nm ± 7 nm without the hydrogen ion implantation so that it was confirmed that the thickness distribution was deteriorated due to influence of dispersion of thicknesses of porous silicon.

[0200]

Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0201]

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50 μm square region was about 0.2 nm which was equal to the silicon wafer on the market.

[0202]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0203]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0204]

At the same time, the porous Si layer remaining on the first Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal

Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed, and the Si substrate could be again put into the porosity-forming process.

[0205]

[Example 9]

Two first p- or n-type (100) single-crystal Si substrates each having 625 μm in thickness, 0.01 Ω•cm in resistivity and 6 inches in diameter were prepared and anodized in an HF solution.

[0206]

The anodization condition was as follows:

[0207]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH = 1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0208]

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the MBE (molecular beam epitaxy) method, single-crystal Si was epitaxial-grown by 0.5 μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

[0209]

Temperature: 700°C

Pressure: 1×10^{-9} Torr

Growing Speed: 0.1 nm/sec

Temperature: 950°C

Growing Speed: 0.3 μm/min

[0210]

Further, an SiO_2 layer of 100 nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0211]

Subsequently, helium ions of $1 \times 10^{17}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100 keV.

[0212]

The surface of the SiO_2 layer and the surface of a separately prepared support Si substrate formed with an SiO_2 layer of 500 nm were overlapped and abutted with each other, and subjected to the heat treatment at 300°C for 2 hours. The bonded two wafers were fixed by a vacuum chuck and applied with torsion and shearing forces in the horizontal direction relative to the main surface of the wafers. Then, the two substrates were completely separated at a position corresponding to the projection range of the helium ion implantation. The separated surfaces were observed in detail using an optical microscope, but exposed portions of the initial bonded interface were not found. On the other hand, when the

pressure was further applied to the substrate (not subjected to the helium ion implantation), the vacuum chuck was detached and the substrate could not be put into the subsequent process.

[0213]

Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

[0214]

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0215]

Specifically, the single-crystal Si layer having 0.1 μm in thickness was formed on the Si oxidized film. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 101 nm ± 3 nm with the hydrogen ion implantation, while it was 101 nm ± 7 nm without the

hydrogen ion implantation so that it was confirmed that the thickness distribution was deteriorated due to influence of dispersion of thicknesses of porous silicon. Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0216]

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50 μm square region was about 0.2 nm which was equal to the silicon wafer on the market.

[0217]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0218]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer. At the same time, the porous Si layer remaining on the first Si substrate side was also agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed, and the Si substrate could be again put into the porosity-forming process.

[0219]

[Example 10]

Two first p- or n-type (100) single-crystal Si substrates each having 625 μm in thickness, 0.01 Ω•cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

[0220]

The anodization condition was as follows:

[0221]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH$ = 1:1:1

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0222]

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.55 μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

[0223]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900°C

Growing Speed: 0.3 μm/min

Further, an SiO_2 layer of 100 nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0224]

Subsequently, hydrogen ions of $1 \times 10^{18}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100 keV.

[0225]

The surface of the SiO_2 layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to increase the bonding strength. Then, the porous Si layer was divided into two at the ion-implanted region.

[0226]

On the other hand, no change was observed at the substrate which was not subjected to the helium ion implantation.

[0227]

Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

[0228]

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0229]

Specifically, the single-crystal Si layer having 0.5 μm in thickness was formed on the quartz substrate. Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501 nm ± 11 nm with the hydrogen ion implantation. Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0230]

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50 μm square region was about 0.2 nm which was equal to the silicon wafer on the market.

[0231]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0232]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0233]

[Example 11]

A first p- or n-type (100) single-crystal Si substrate having 625 μm in thickness, 0.01 Ω•cm in resistivity and 5 inches in diameter was prepared and anodized in an HF solution.

[0234]

The anodization condition was as follows:

[0235]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH$ = 1:1:1

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0236]

The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the MOCVD (metal organic chemical vapor deposition) method, single-crystal GaAs was epitaxial-grown by 1 μm on porous Si. The growing condition was as follows.

[0237]

Source Gas: $TMG/AsH_3/H_2$

Gas Pressure: 80 Torr

Temperature: 700°C

[0238]

Subsequently, helium ions of $1 \times 10^{18}/cm^2$ were implanted into the porous side of the substrate at acceleration voltage of 100 keV.

[0239]

The surface of the GaAs layer and the surface of a separately prepared support Si substrate were overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to enhance the bonding strength. Then, the porous Si layer was divided into two at the ion-implanted region.

[0240]

Thereafter, after removing the oxidized film on the inner walls of the porous Si layer using hydrofluoric acid, the porous Si was etched with a solution of ethylenediamine, pyrocatechol and water (ratio: 17ml:3g:8ml) at 110°C. Single-crystal GaAs remained without being etched so that porous Si was selective-etched using single-crystal GaAs as etching stopper and fully removed.

[0241]

The etching speed of single-crystal GaAs relative to the etching liquid is extremely low so that the thickness reduction can be ignored from a practical point of view.

[0242]

Specifically, the single-crystal GaAs layer having 1 μm in thickness was formed on the Si substrate. No change was caused on the single-crystal GaAs layer even by the selective etching of porous Si.

[0243]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the GaAs layer and the excellent crystallinity was maintained.

[0244]

By using the Si substrate with the oxidized film as the support substrate, GaAs on the insulating film could also be produced similarly.

[0245]

[Example 12]

A first p- or n-type (100) single-crystal Si substrate having 625 μm in thickness, 0.01Ω•cm in resistivity and 5 inches in diameter was prepared and anodized in an HF solution.

[0246]

The anodization condition was as follows:

[0247]

Current Density: 10 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH = 1:1:1$

Time: 24 (minutes)

Thickness of Porous Si: 20 (μm)

Porosity: 17 (%)

[0248]

The substrate was oxidized at 400°C in the oxygen atmosphere for 2 hours. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the MBE (molecular beam epitaxy) method, single-crystal AlGaAs was epitaxial-grown by 0.5 μm on porous Si.

[0249]

Subsequently, helium ions of $1 \times 10^{18}/cm^2$ were implanted into the porous side of the substrate at acceleration voltage of 100 keV.

[0250]

The surface of the AlGaAs layer and the surface of a separately prepared support substrate of low melting point glass were overlapped and abutted with each other, and subjected to the heat treatment at 500°C for 2 hours. Through this heat treatment, the substrates were firmly bonded with each other.

[0251]

When the sufficient pressure was applied to the bonded wafers perpendicularly relative to the in-plane and uniformly over the in-plane, the porous Si layer was divided into two at the ion-implanted region.

[0252]

Thereafter, porous Si was etched with a hydrofluoric acid solution. Single-crystal AlGaAs remained without

being etched so that porous Si was selective-etched using single-crystal AlGaAs as etching stopper and fully removed.

[0253]

The etching speed of single-crystal AlGaAs relative to the etching liquid is extremely low so that the thickness reduction can be ignored from a practical point of view.

[0254]

Specifically, the single-crystal AlGaAs layer having 0.5 μm in thickness was formed on the glass substrate. No change was caused on the single-crystal AlGaAs layer even by the selective etching of porous Si.

[0255]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the AlGaAs layer and the excellent crystallinity was maintained.

[0256]

[Example 13]

A first p- or n-type (100) single-crystal Si substrate with both sides polished and having 625 μm in thickness, 0.01 Ω•cm in resistivity and 6 inches in diameter was prepared and anodized at both sides thereof in an HF solution.

[0257]

The anodization condition was as follows:

[0258]

Current Density: 5 ($mA \cdot cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH$ = 1:1:1

Time: 12 × 2 (minutes)

Thickness of Porous Si: 10 (μm) for each side

Porosity: 15 (%)

[0259]

The substrate was oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 1 μm on porous Si formed at each side. The growing condition was as follows.

[0260]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 950°C

Growing Speed: 0.3 μm/min

[0261]

Further, an SiO_2 layer of 100 nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0262]

Subsequently, hydrogen ions of $1 \times 10^{18}/cm^2$ were implanted into the porous layers at acceleration voltage

of 100 keV.

[0263]

The surfaces of the SiO_2 layers and the surfaces of separately prepared two support Si substrates each formed with an SiO_2 layer of 500 nm were overlapped and abutted with each other, and subjected to the heat treatment at 600°C for 2 hours so as to achieve bonding. Then, the porous Si layer was divided into two at the ion-implanted region.

[0264]

Thereafter, the porous Si layer was agitated in a mixed solution (1:5) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

[0265]

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0266]

Specifically, the two single-crystal Si layers each having 1 μm in thickness were simultaneously formed on

the Si oxidized films. No change was caused on the single-crystal Si layers even by the selective etching of porous Si.

[0267]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0268]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0269]

[Example 14]

Two first p- or n-type (100) single-crystal Si substrates each having 625 μm in thickness, 0.01 Ω∘cm in resistivity and 5 inches in diameter were prepared and anodized in an HF solution.

[0270]

The anodization condition was as follows:

[0271]

Current Density: 5 ($mA \circ cm^{-2}$)

Anodization Solution: $HF:H_2O:C_2H_5OH = 1:1:1$

Time: 12 (minutes)

Thickness of Porous Si: 10 (μm)

Porosity: 15 (%)

[0272]

The substrates were oxidized at 400°C in the oxygen atmosphere for 1 hour. Through the oxidation, the pore inner walls of porous Si were coated with thermal-oxidized films. Using the CVD (chemical vapor deposition) method, single-crystal Si was epitaxial-grown by 0.55 μm on porous Si. The growing condition was as follows. The accuracy of the film thickness was ±2%.

[0273]

Source Gas: SiH_2Cl_2/H_2

Gas Flow Rate: 0.5/180 l/min

Gas Pressure: 80 Torr

Temperature: 900°C

Growing Speed: 0.3 μm/min

[0274]

Further, an SiO_2 layer of 100 nm was formed on the surface of each epitaxial Si layer through thermal oxidation.

[0275]

Subsequently, hydrogen ions of $1 \times 10^{18}/cm^2$ were implanted into the porous side of only one of the substrates at acceleration voltage of 100 keV.

[0276]

The surface of the SiO_2 layer and the surface of a separately prepared support quartz substrate were exposed to oxygen plasma, respectively, then overlapped and abutted with each other, and subjected to the heat treatment at 200°C for 2 hours so as to increase the

bonding strength. Subsequently, the wave energy such as the ultrasonic wave was applied to the substrates. Then, the porous Si layer was divided into two at the ion-implanted region.

[0277]

On the other hand, no change was observed at the substrate which was not subjected to the hydrogen ion implantation.

[0278]

Thereafter, the porous Si layer remaining on the second substrate side was agitated in a mixed solution (1:2) of 49% hydrofluoric acid and 30% aqueous hydrogen peroxide for selective etching. Single-crystal Si remained without being etched so that porous Si was selective-etched using single-crystal Si as etching stopper and fully removed.

[0279]

The etching speed of non-porous single-crystal Si relative to the etching liquid is extremely low so that the selection ratio relative to the etching speed of the porous layer reaches as much as no less than 10^5 and the etching amount (about several tens of angstroms) at the non-porous layer can be ignored from a practical point of view.

[0280]

Specifically, the single-crystal Si layer having 0.5 μm in thickness was formed on the quartz substrate.

Thicknesses of the formed single-crystal Si layer were measured at 100 points thereover. Uniformity of the thicknesses was 501 nm ± 11 nm with the hydrogen ion implantation. Thereafter, the heat treatment was performed at 1,100°C in the hydrogen atmosphere for 1 hour.

[0281]

When evaluating the surface roughness using an interatomic force microscope, the mean square roughness at a 50 μm square region was about 0.2 nm which was equal to the silicon wafer on the market.

[0282]

As the result of section observation by a transmission electron microscope, it was confirmed that no new crystal defects were introduced into the Si layer and the excellent crystallinity was maintained.

[0283]

Similar results were obtained even without forming the oxidized film on the surface of the epitaxial Si layer.

[0284]

The first single-crystal Si substrate was reused as a single-crystal Si substrate after removing remaining porous Si and performing surface-polishing to provide a mirror finished surface.

[0285]

[Effect of the Invention]

As described above in detail, according to the present invention, there are provided a semiconductor substrate and a forming method thereof which can solve the foregoing various problems and satisfy the above requirements.

[0286]

As described above in detail, according to the present invention, there are provided a semiconductor substrate and a forming method thereof which can solve the foregoing various problems by superimposing a fine porous structure in a porous layer.

[0287]

According to the present invention, a structure can easily be formed, wherein a porous layer having a fine structure to act as a luminescent material is sandwiched in a porous layer having a high mechanical strength. Accordingly, although the porous layer having such a fine structure differs from bulk Si in lattice constant, by sandwiching it in the large porous Si layer having intermediate lattice constant, stresses can be relaxed and introduction of cracks or defects can be suppressed. Specifically, since the luminescent layer which is stable in structure can be formed, it is not only possible to serve for formation of peripheral circuit or wiring, but also possible to provide a material which is excellent in long-term stability.

[0288]

According to the present invention, since an extremely thin porous substrate corresponding to a projection range of ion implantation can be formed, when using said substrate as a filter for particles in gases, it is possible to produce a filter which can remove the particles greater than several tens of nanometers in diameter and whose pressure loss is small. Further, if high purity Si which is used in the semiconductor process is used as a substrate, there is no worry about contamination from the filter itself.

[0289]

Further, when the method of the present invention is used, after separation of the porous substrate, the first Si substrate can be reused. Also, the first Si substrate can repeatedly be reused until it can not be used relating to its strength.

[0290]

According to the present invention, since the porous layer of a fine structure can be formed after formation of the single-crystal silicon layer on the porous layer, the epitaxial growth condition of the single-crystal layer can be set free of influence of the structural change of the porous layer. Specifically, since the fine-structure porous layer, working as a luminescent layer, which tends to change due to thermal treatment, can be formed after completion of thermal treatment for the film formation, the characteristic of the element can

be stable.

[0291]

According to the present invention, upon removal of the first Si substrate, the Si substrate can be separated at one time in large area via the porous layer. If the separated first Si substrate is rough in a degree such that its surface flatness is not allowable after removing the remaining porous layer, the first Si substrate is subjected to a surface flattening treatment and then can be reused as a first Si substrate. Further, the first Si substrate can repeatedly be reused until it can not be used relating to its strength.

[0292]

According to the present invention, by previously ion implanting at least one element of rare gases, hydrogen and nitrogen into the porous layer with a given projection range, the Si substrate can be separated in advance at one time in large area via the porous layer. Thus, the grinding, polishing or etching process which was essential in the prior art for removing the Si substrate to expose the porous silicon layer can be omitted to shorten the process. Further, since the separating position is limited to within the porous layer with large porosity by implanting ions of at least one kind of rare gases, hydrogen and nitrogen into the porous layer so as to have the projection range, thicknesses of the porous layer remaining on the second substrate side

can be uniform so that the porous layer can be removed with excellent selectivity. In the conventional method of producing the bonded substrates, the first Si substrate is gradually removed from one side thereof through grinding or etching. Thus, it is impossible to effectively use both sides of the first Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the first Si substrate is held in the initial state other than its surface layers so that, by using both sides of the first Si substrate as the main surfaces and bonding the support substrates to the sides of the Si substrate, respectively, two bonded substrates can be simultaneously produced from one first Si substrate.

[0293]

According to the present invention, upon removal of the Si substrate, since the Si substrate can be separated at one time in large area via the porous layer, the process can be shortened. Further, since the separating position is limited to within the porous layer by means of the ion implantation, thicknesses of the porous layer remaining on the second substrate side can be uniform so that the porous layer can be removed with high selectivity. Thus, even when the etching is unstable due to the size of the apparatus or the change of the environment, the non-porous thin film, such as the single-crystal Si layer or the compound semiconductor

single-crystal layer, which is excellent in economics, flat and uniform over the large area and has the extremely excellent crystallinity, can be transferred onto the second substrate with high yield. Specifically, the SOI structure with the single-crystal Si layer formed on the insulating layer can be obtained with high uniformity of film thickness and high yield. Further, since the separating position is regulated by the projection range of the ion implantation so as to be within the porous layer, the thicknesses of the porous layer remaining on the second substrate side can be uniform so that the porous layer can be removed with high selectivity. Namely, the grinding or etching process which was essential in the prior art for exposing the porous silicon can not only be omitted, but also the separated first Si substrate can be reused as a first Si substrate by removing the remaining porous layer. If the surface flatness is insufficient of the Si substrate after removing the porous layer, a surface flattening treatment is performed. Since the separation site of the bonded two substrates is determined by the projection range, the separation site does not disperse different from the prior art. Therefore, upon removal of the porous silicon, it does not happen that the easier exposed single-crystal silicon layer is etched to deteriorate the film thickness uniformity. Further, the first Si substrate can repeatedly be reused until it can

not be used relating to its strength. Further, since the separation site of the substrates is limited to near the depth corresponding the projection range of ion implantation, the thickness of the porous layer can be thin compared with that of the prior art.

[0294]

Alternatively, without removing the remaining porous layer, the separated first Si substrate can be reused again as a first Si substrate of the present invention by again forming a non-porous single-crystal Si layer. Also in this case, the first Si substrate can be reused in the desired number of times until its structural strength makes it impossible.

[0295]

In the conventional method of producing the bonded substrates, the first Si substrate is gradually removed from one side thereof through grinding or etching. Thus, it is impossible to effectively use both sides of the first Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the first Si substrate is held in the initial state other than its surface layers so that, by using both sides of the first Si substrate as the main surfaces and bonding the support substrates to the sides of the Si substrate, respectively, two bonded substrates can be simultaneously produced from one first Si substrate. Thus, the process can be shortened and the productivity can be improved.

As appreciated, also in this case, the separated first Si substrate can be recycled as an Si substrate.

[0296]

Further, according to the process for preparing a semiconductor substrate of the present invention, after removing the remaining porous layer, the first Si substrate separated by the foregoing method may be reused as a first Si substrate by performing the surface flattening process if the surface flatness property is insufficient. The surface flattening process may be polishing, etching or the like normally used in the semiconductor process. On the other hand, the heat treatment in the atmosphere including hydrogen may also be used. By selecting the condition, the heat treatment can achieve the flatness to an extent where the atomic step is locally presented.

[0297]

Specifically, the present invention uses a single-crystal Si substrate which is excellent in economics, flat and uniform over a large area and has an extremely excellent crystallinity, and removes from one side thereof to an Si or compound semiconductor active layer formed on the surface which thus remains, so as to provide a single-crystal Si layer or a compound semiconductor single-crystal layer with extremely less defects on an insulating material.

[0298]

The present invention provides a producing method of a semiconductor substrate which is capable of achieving an Si or compound semiconductor single-crystal layer with a crystallinity as good as a single-crystal wafer on a transparent substrate (light transmissible substrate), with high productivity, high uniformity, excellent controllability and reduced cost.

[0299]

According to the producing method of the semiconductor substrate of the present invention, since the selective etching which is excellent in a ratio of etching selectivity can be performed, the Si single crystal or the compound semiconductor single crystal on the support substrate, which is flat and uniform over the large area and has an extremely excellent crystallinity, can be obtained.

[0300]

Further, since porous Si has a low mechanical strength and an extensive surface area, removal of the porous Si layer of the present invention can also be performed by selective polishing using the single-crystal layer as a polishing stopper.

[0301]

Specifically, the present invention uses a single-crystal Si substrate which is excellent in economics, flat and uniform over a large area and has an extremely excellent crystallinity, and removes from one side

thereof to an Si or compound semiconductor active layer formed on the surface which thus remains, so as to provide a single-crystal Si layer or a compound semiconductor single-crystal layer with extremely less defects on an insulating material.

[0302]

The present invention provides a producing method of a semiconductor substrate which is capable of achieving an Si or compound semiconductor single-crystal layer with a crystallinity as good as a single-crystal wafer on a transparent substrate (light transmissible substrate), with high productivity, high uniformity, excellent controllability and reduced cost.

[0303]

Further, the present invention provides a producing method of a semiconductor substrate which is replaceable for an expensive SOS or SIMOX upon producing a large scale integrated circuit of an SOI structure.

[0304]

According to the present invention, the single-crystal compound semiconductor layer with excellent crystallinity can be formed on porous Si, and further, this semiconductor layer can be transferred onto the large-area insulating substrate which is excellent in economics. Thus, the foregoing problem of the difference in lattice constant and thermal expansion coefficient can be sufficiently suppressed so as to form the compound

semiconductor layer with excellent crystallinity on the insulating substrate.

[0305]

According to the present invention, the single-crystal compound semiconductor layer with excellent crystallinity can be formed on porous Si, and further, this semiconductor layer can be transferred onto the large-area insulating substrate which is excellent in economics. Thus, the foregoing problem of the difference in lattice constant and thermal expansion coefficient can be sufficiently suppressed so as to form the compound semiconductor layer with excellent crystallinity on the insulating substrate.

[0306]

Further, even if non-formation regions of the implanted layer are formed due to presence of the foreign matter on the surface upon the ion implantation, since the mechanical strength of the porous layer itself is smaller than bulk Si, the separation occurs in the porous layer. Thus, the bonded two substrates can be separated without causing damages such as cracks in the non-porous single-crystal silicon layer.

[0307]

Further, after selectively removing the porous silicon layer remaining on the surface of the separated substrate by a method such as etching and polishing, the single-crystal silicon layer can be transferred on the

second substrate. Further, after removing the remained porous silicon from the first substrate, a porous silicon layer and a single-crystal silicon layer are again formed on the first substrate, and ion implantation of at least one element of rare gases, hydrogen and nitrogen into the porous layer with a given projection range is conducted, and then the first substrate can be bonded to a second substrate. Namely, the first substrate can be reused. Further, when the first substrate is heat-treated in a reducing atmosphere such as an atmosphere containing hydrogen in a state that the porous layer is remained on the first substrate, the surface of the porous silicon layer is flattened, thereby a single-crystal silicon layer can be formed on the first substrate. When the single-crystal silicon layer is bonded to a second substrate, the first substrate can be reused.

[0308]

Further, since the gettering effect is available at the ion-implanted region, even if metal impurities exist, the bonded two substrates are separated after achieving the gettering of the impurities into the ion-implanted region, and then the ion-implanted region is removed so that it is also effective against the impurity contamination.

[0309]

According to the method of the present invention, since the separating region is limited to the ion-

implanted region within the porous layer, the depths of the separating region do not disperse within the porous layer. Accordingly, even if the ratio of etching selectively of porous silicon is insufficient, a time for removing porous silicon can be rendered substantially constant so that the thickness uniformity of the single-crystal silicon layer transferred onto the support substrate is not spoiled.

[0310]

In the conventional method of producing the bonded substrates, the first Si substrate is gradually removed from one side thereof through grinding or etching. Thus, it is impossible to effectively use both sides of the first Si substrate for bonding to the support substrate. On the other hand, according to the present invention, the first Si substrate is held in the initial state other than its surface layers so that, by using both sides of the first Si substrate as the main surfaces and bonding the support substrates to the sides of the Si substrate, respectively, two bonded substrates can be simultaneously produced from one first Si substrate. As appreciated, also in this case, the separated first Si substrate can be recycled as an first Si substrate.

[Brief Description of the Drawings]

[Fig. 1]

A schematic view for explaining one example of process steps for producing a semiconductor substrate

according to the present invention.

[Fig. 2]

A schematic view for explaining another example of process steps for producing a semiconductor substrate according to the present invention.

[Fig. 3]

A schematic view for explaining further example of process steps for producing a semiconductor substrate according to the present invention.

[Fig. 4]

A schematic view for explaining further example of process steps for producing a semiconductor substrate according to the present invention.

[Fig. 5]

A schematic view for explaining further example of process steps for producing a semiconductor substrate according to the present invention.

[Fig. 6]

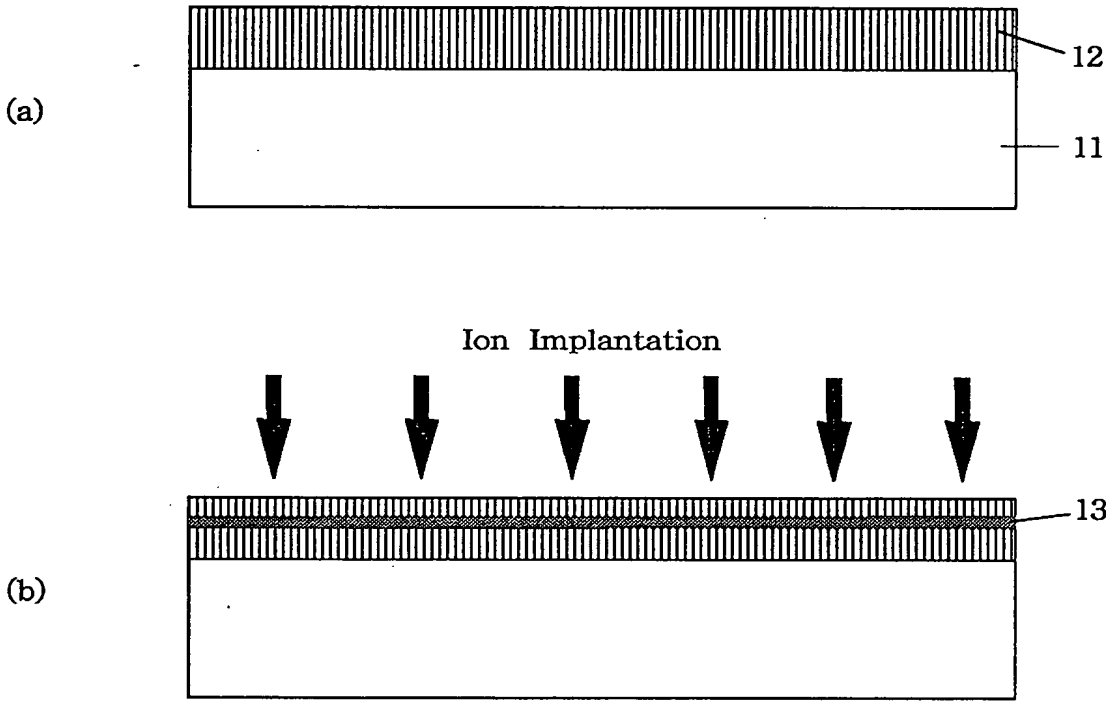
A schematic view for explaining one example of process steps for producing a semiconductor substrate which has been proposed before by the applicants.

[Fig. 7]

A schematic view for explaining an example of process steps for producing a semiconductor substrate according to a conventional method.

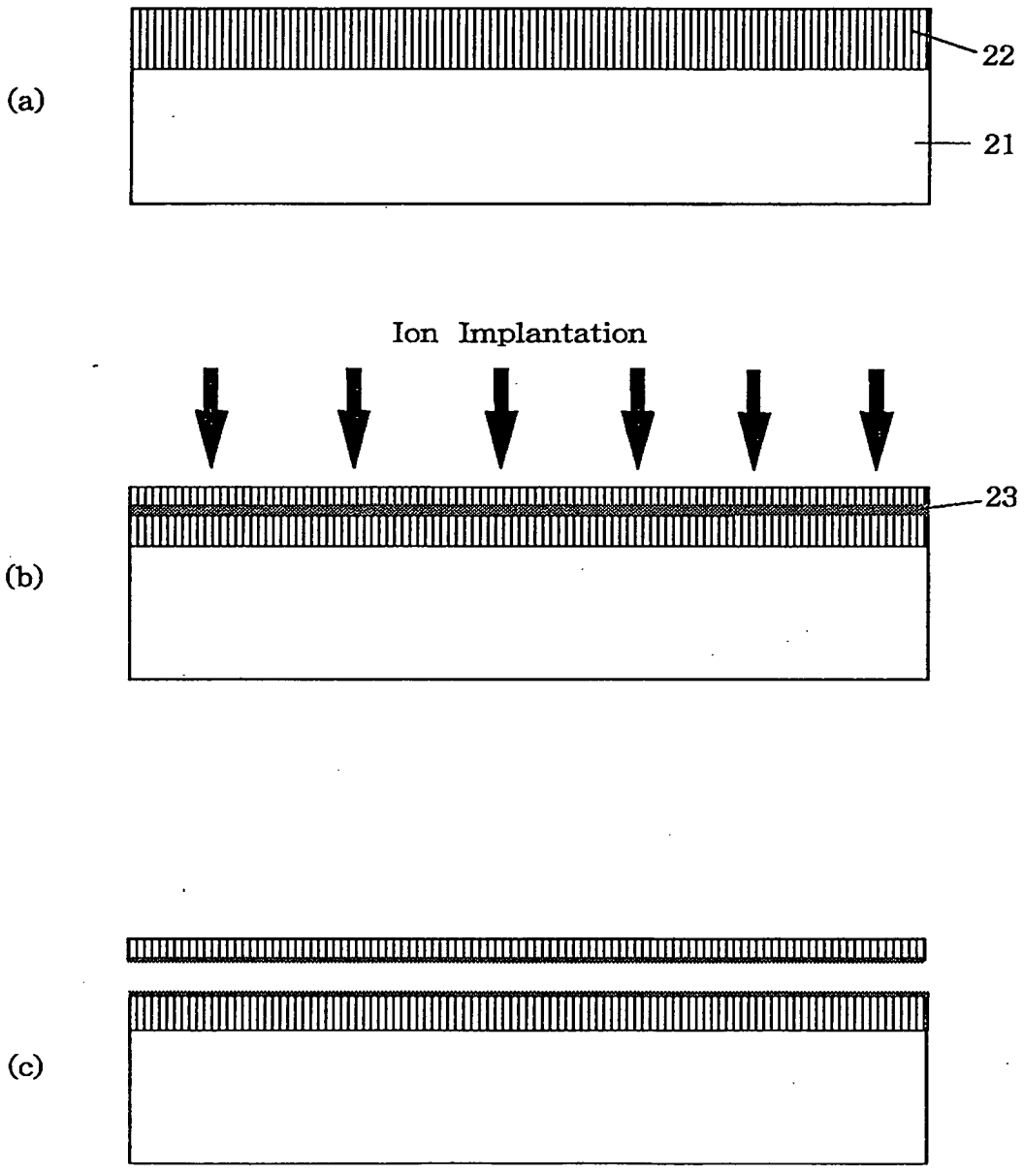
【書類名】　図面

【図１】　Fig. 1



【図２】

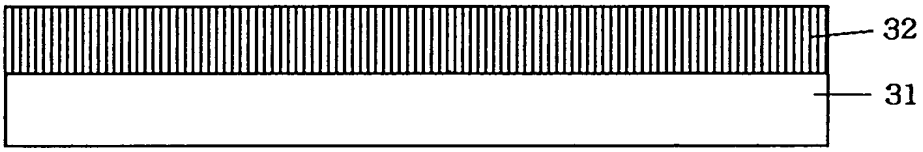
Fig. 2



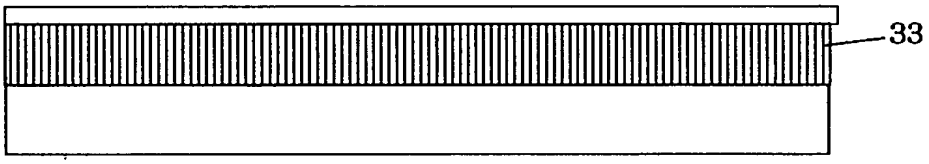
【図３】

Fig. 3

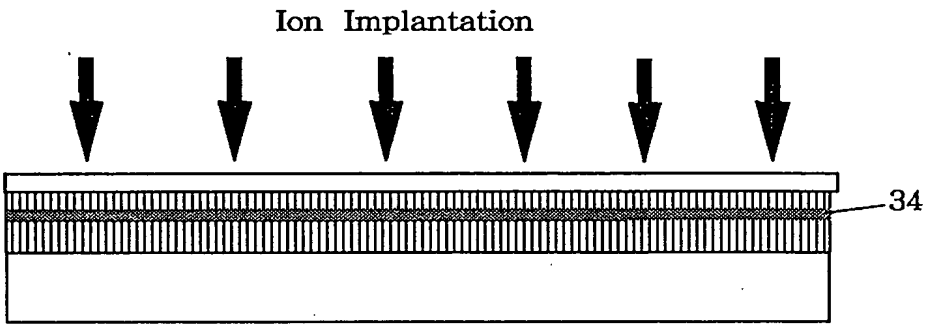
(a)



(b)

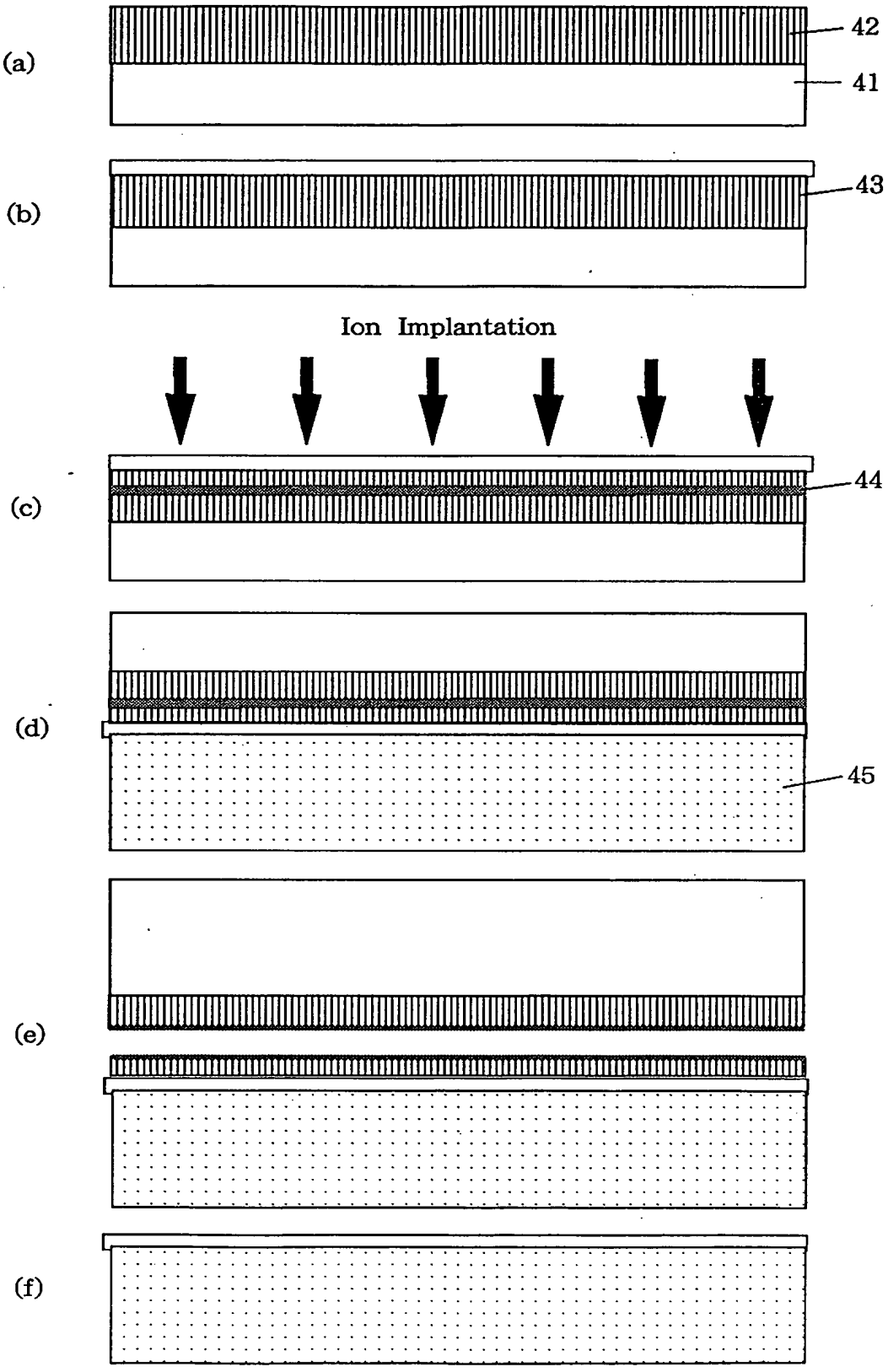


(c)

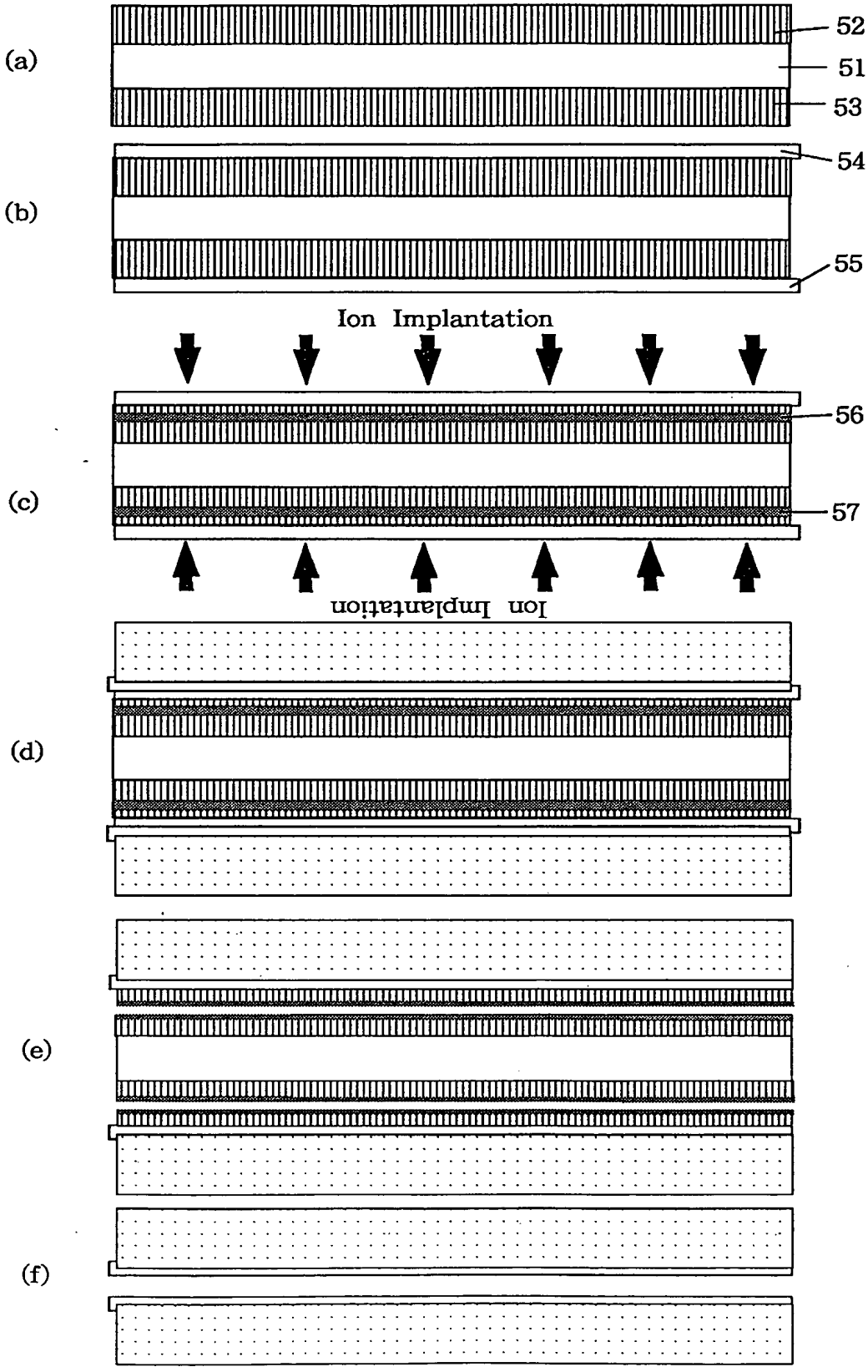


【図４】

Fig. 4

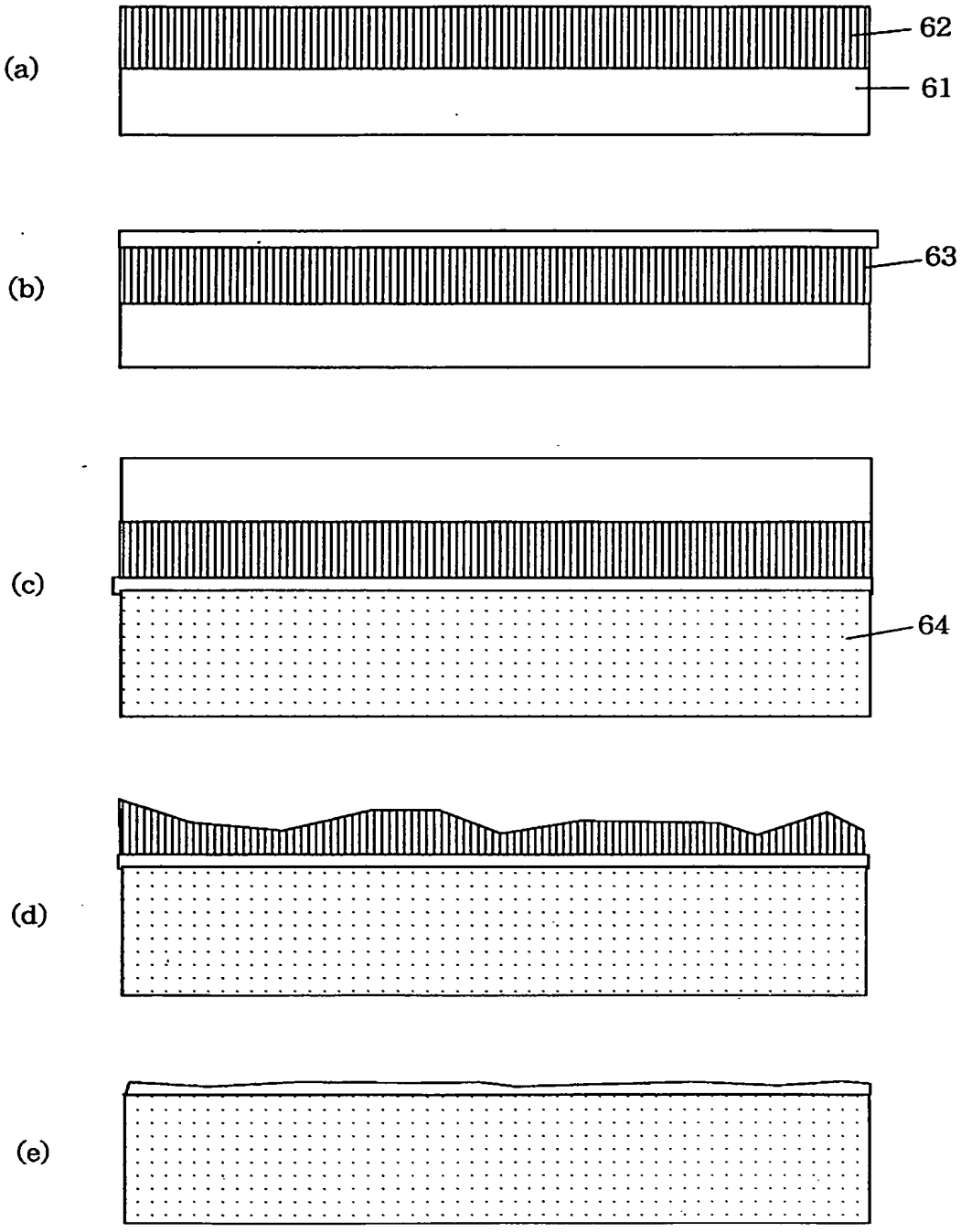


【図５】　Fig. 5

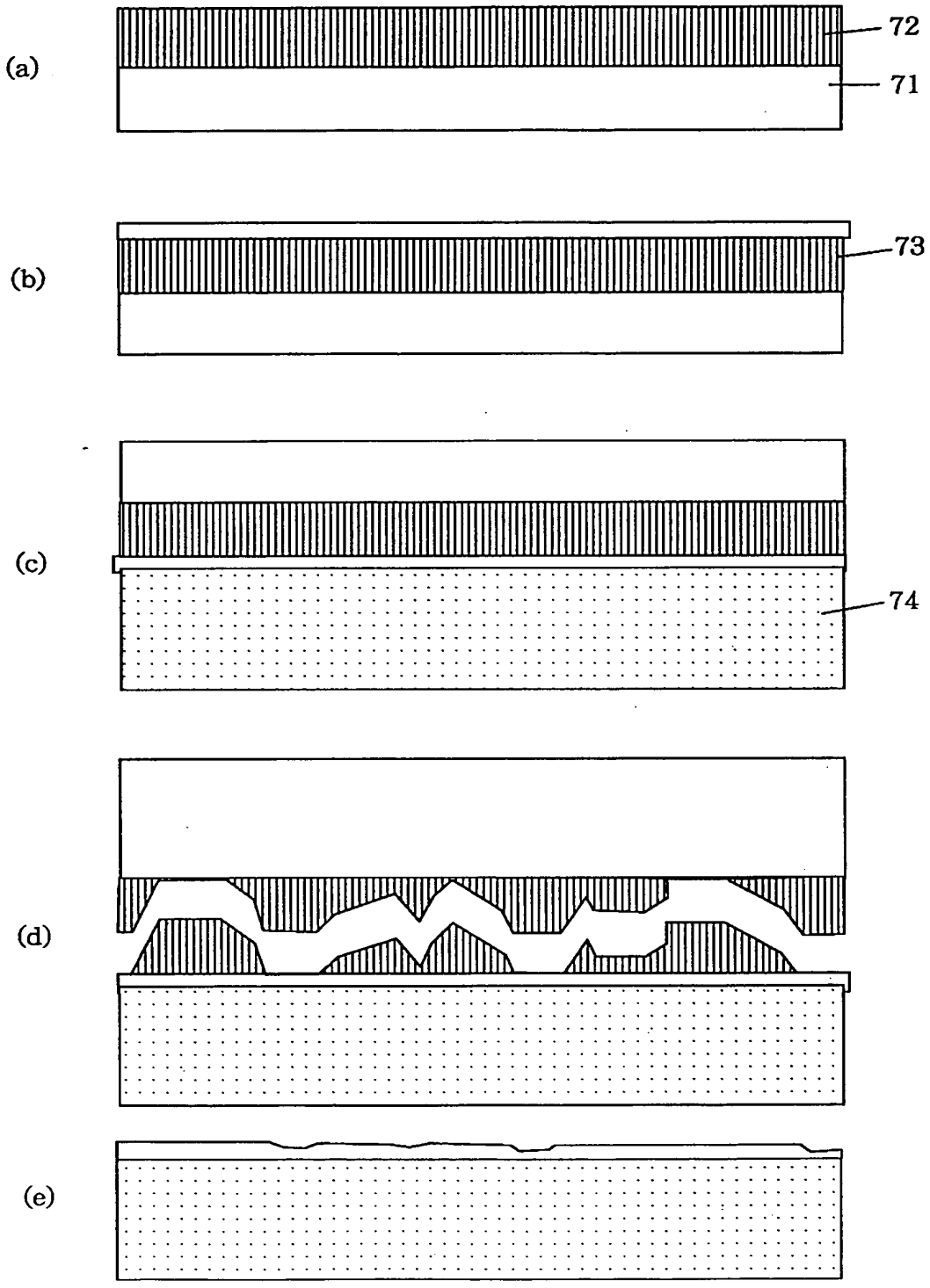

(a)
52
51
53
(b)
54
55
Ion Implantation
(c)
56
57
Ion Implantation
(d)
(e)
(f)

【図６】

Fig. 6



【図７】　Fig. 7



[Name of the Document]

Abstract

[Abstract]

[Problem]

There is provided a method for producing an SOI substrate having a high quality with high reproducibility and simultaneously for achieving resources saving and reduction in cost through recycling of the wafer.

[Means for Solving the Problem]

A semiconductor substrate comprising a porous Si layer as a surface layer of at least one main plane side of an Si substrate and a porous Si layer having a thin pore wall included in said porous Si layer.

[Elected Drawing]

Fig. 1

[Name of the Document] Authorized Correction Data

[Document to be corrected] Patent Application

<Recognition Information • Additional Information>

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1. Date of Change: August 30, 1990

(Reason for Change) New Registration

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